ESD-related damage mechanisms in microelectronic devices

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ESD praktijkdag, Amsterdam, November 04, 2014

Overview about ESD damages caused by process robotics

- MM- and CDM- based ESD-damages via pins (from wafer level to PCB)
- Memory loss (from wafer to encapsulated device)
- BS-ESD-induced cracking (die Pick&Place)
- Reverse-bias leakage enhancement (mainly LEDs)
- Obstructions in the process sequence by "electrostatic adhesion", getting stucked etc…
- ESDFOS (from wafer to encapsulated device/ COB)

ESD damage introduced via pins/ pads

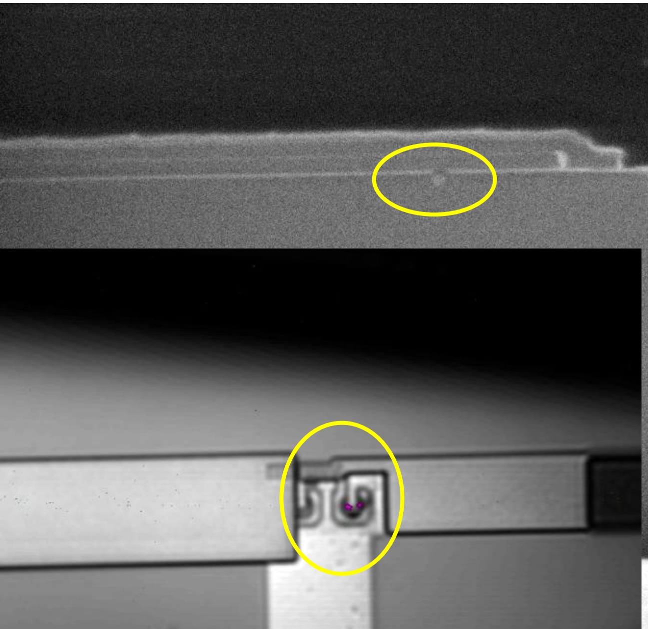
- introduction paths: via pads (wafer/ dice) or pins (capsulated chip/ PCB)
- discharge direction and –strength depends from the situation; model assumptions HBM, HMM, MM, CDM, Charged Board Event (CBE) , Cable Discharge Event (CDE)

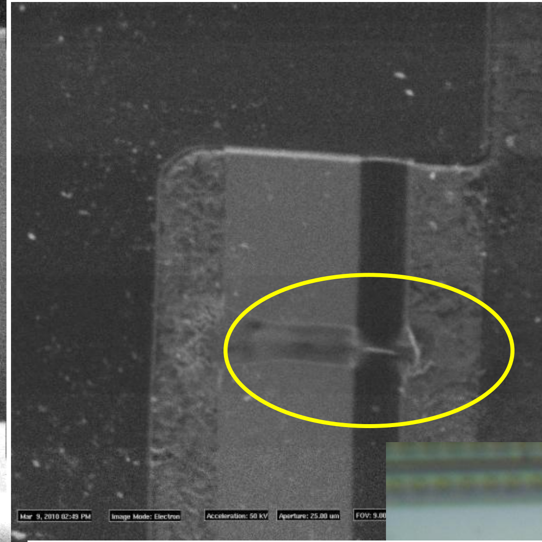
Real World ESD vs. ESD Models

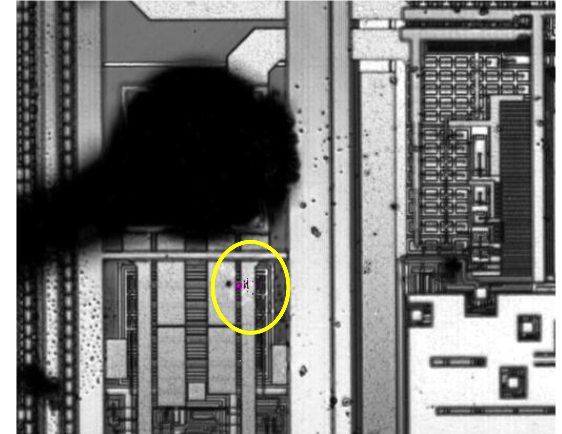
- Pre-discharge (as Corona) consumes energy and falsifies ESD-pulse (applies for all models)
- Geometry of test head influences on Corona effects
- CDM: Mounting of devices (housing/ sockets) severely influences the capacitance
- CBE: Size/ Capacitance of PCB, distance ESDS-pins-to-PCB-terminals and their external protection circuitry
- CDE: Length, capacitance of cable
- MM: Capacitance of machinery part, surface resistance/ dissipativity
- Surface ESD (ESDFOS) not covered by existing models

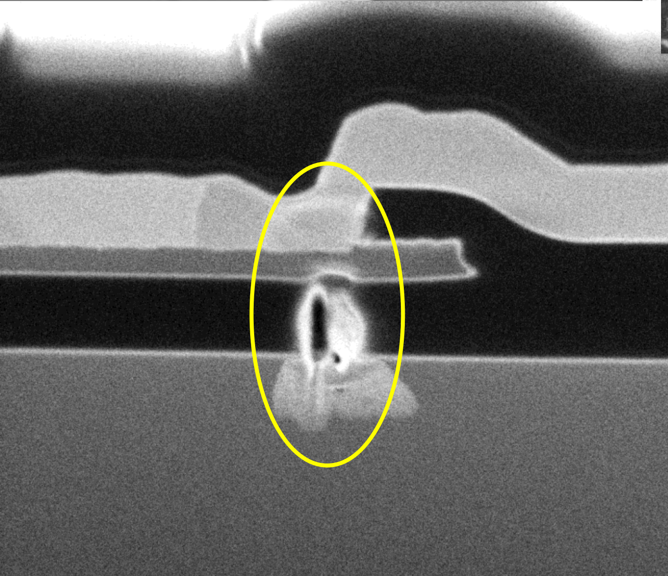
ESD Models can show up discharge mecha-nisms but cannot reflect 100% real-world ESD!

Examples for pin-pathed ESD-damages…

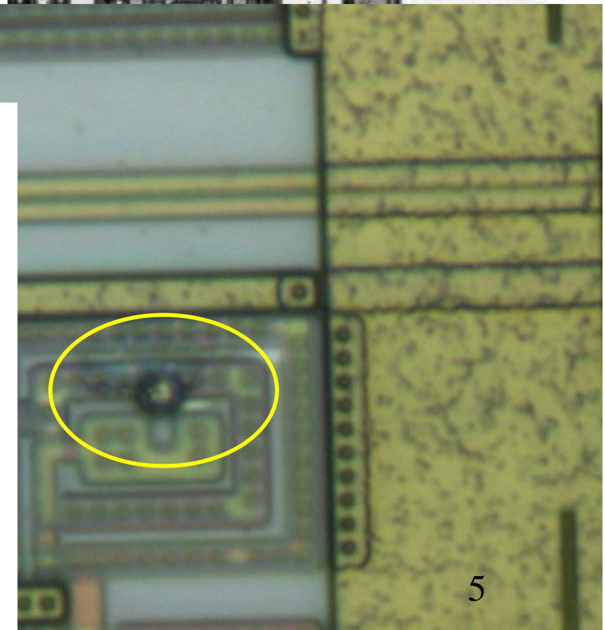








…from hardly detectable p/n leakage to EOS-like breakdowns, frequently assigned by secondary damages, like for instance fused metal lines



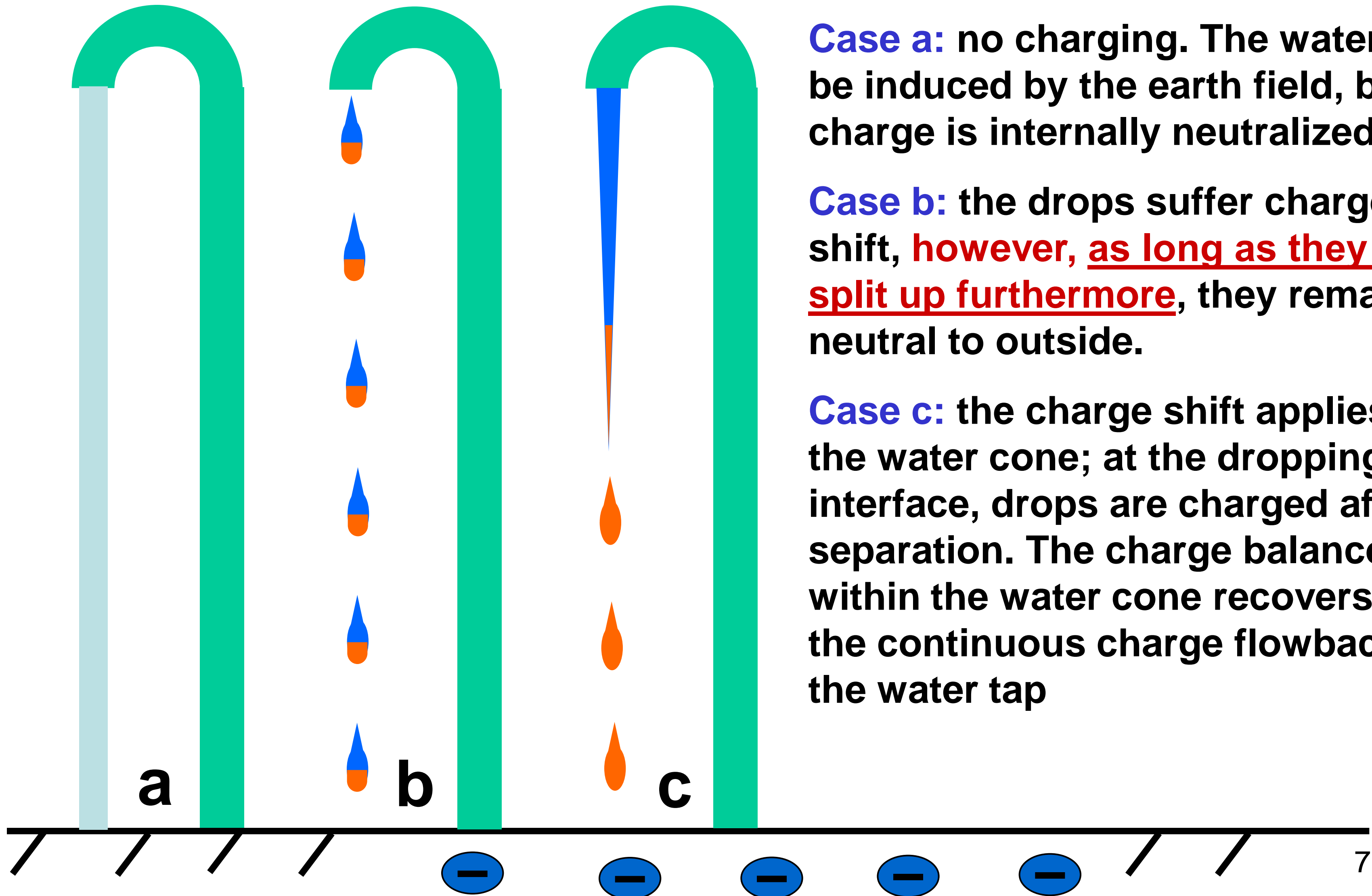
Erasing of EEPROMs by electro-static charging during wafer sawing

Assembly Lot Nr:	Lot 1 (w/o CO_2)	Lot 2 (w/o CO_2)	Lot 3 (w/o CO_2)	Lot 4 (with CO_2)
# Chips	4661	4880	1975	10427
# Chips with erased EEPROM	2293	1406	1054	0
failures %	49%	29%	53%	0%

The improvement achieved by use of CO_2-water is not based on the better electrical conductivity but on the geometrical changes of the spraying behavior.

Wafer Sawing: Charge separation in water drops

++++++++++++Electric Field of the Earth about 130V/m+++++++++++++

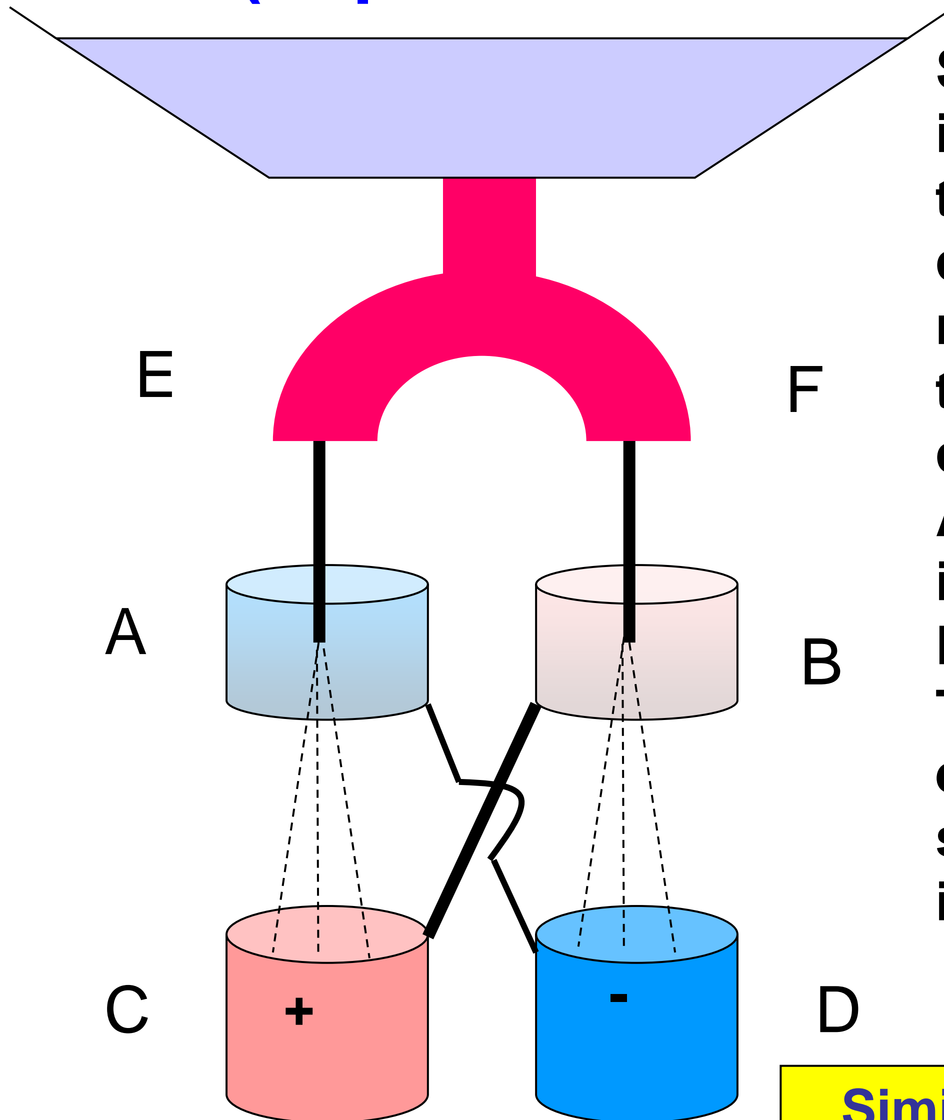


Case a: no charging. The water will be induced by the earth field, but the charge is internally neutralized.

Case b: the drops suffer charge shift, **however, <u>as long as they don‘t split up furthermore</u>**, they remain neutral to outside.

Case c: the charge shift applies to the water cone; at the dropping interface, drops are charged after separation. The charge balance within the water cone recovers by the continuous charge flowback into the water tap

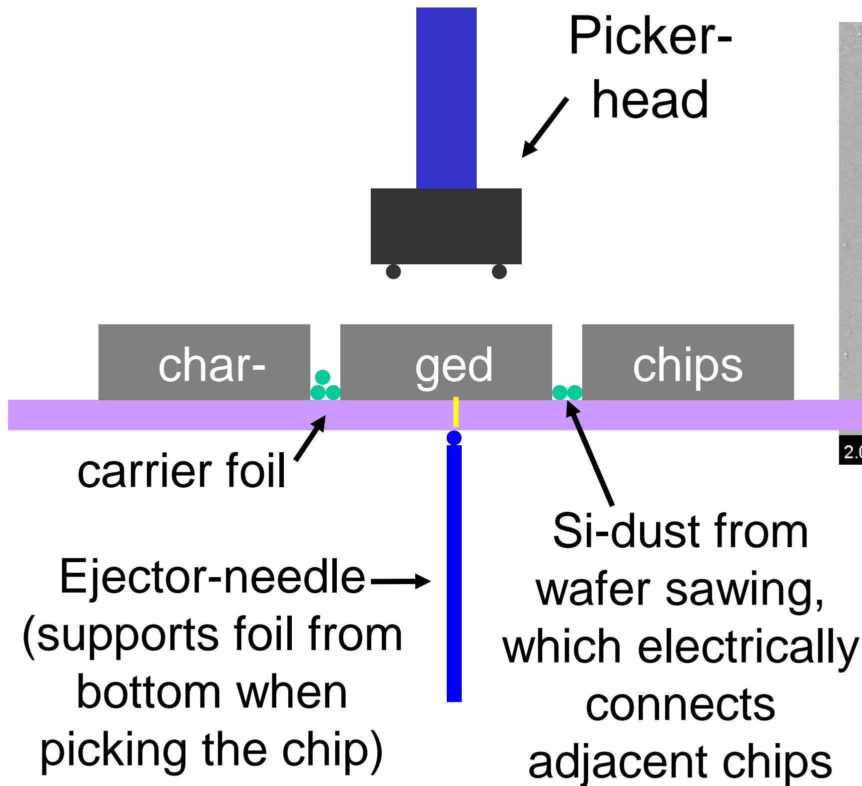
Electrostatic induction in a Kelvin generator
(Experimental demo in the break)



Slightly different dropping rates in A and B generate a small potential difference between the collecting pots C and D, generating a horizontal E-Field between them. By means of cross-circuiting it, using the cylinders A and B, this E-field is converted into two vertical contradictional E-fields between A-C resp. B-D. These fields superimpose the earth E-field and amplify themselves rapidly by electrostatic induction feedback

Similarities in wafer-dicing, cleaning and sand-blasting!

ESD-impacts from the backside when picking chips from the blue carrier foil

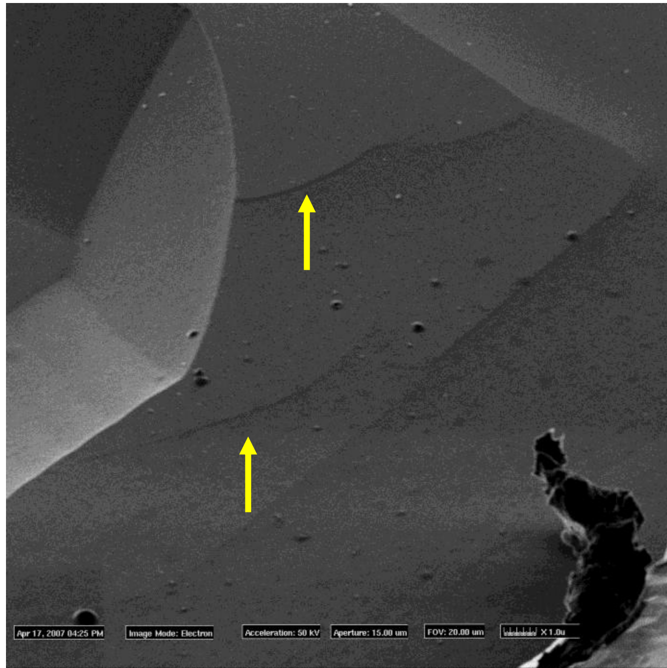


comparison ESD (left) vs. mechanical (right)

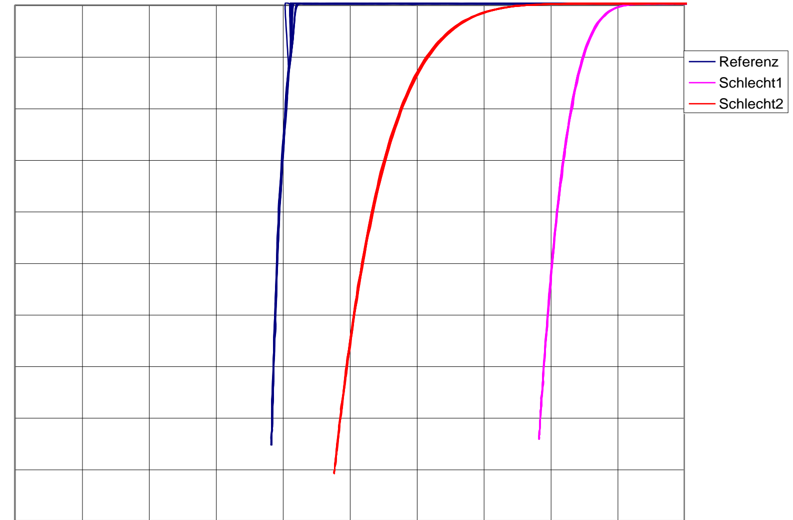
In case of severe damaging, potential bulk crystal damage is generated. Later this may result in die-cracks

crack propagation along crystal axis

ESD damage on LEDs



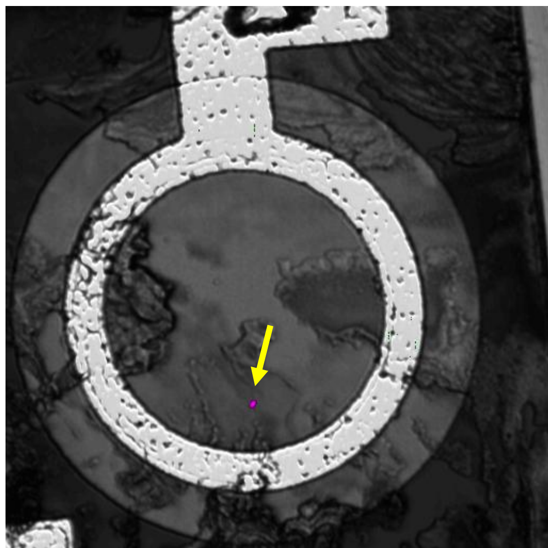
1µA/ div



2V/div →

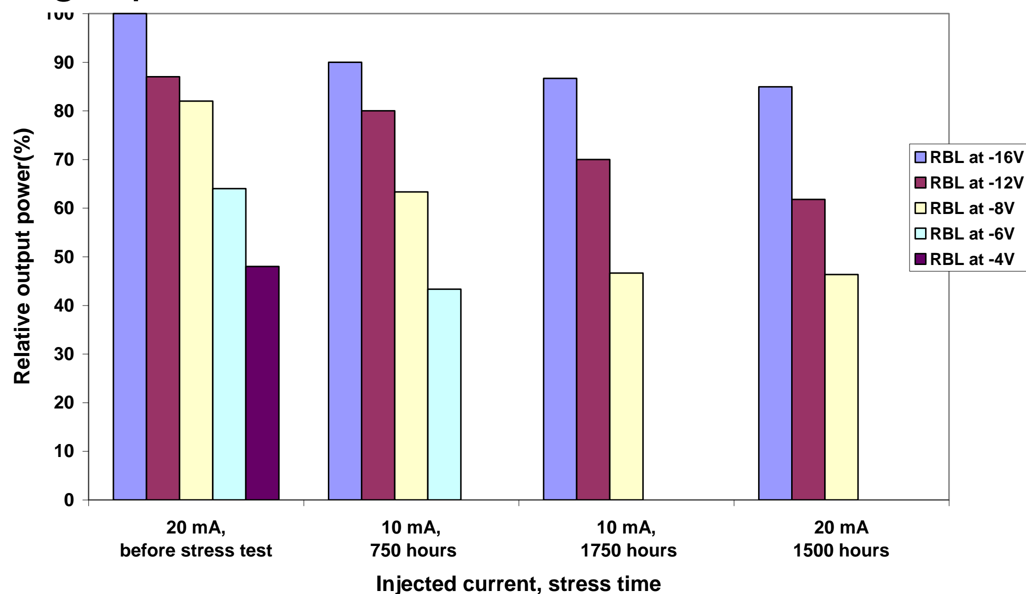
It is hardly known that LEDs are very ESD sensitive. If overvoltage spikes are applied in reverse bias direction, point- ot line-shaped low-current leakage paths are generated. However, since they have a high current density, they start to extend soon, Since they are superimposed in the forward direction by the low-voltage operational IV-characteristics, they remain without attracting attention at first. However, they shorten the LED lifetime significantly in by-the-time formation of dark lines and dark spots, thus reducing the emitted light.

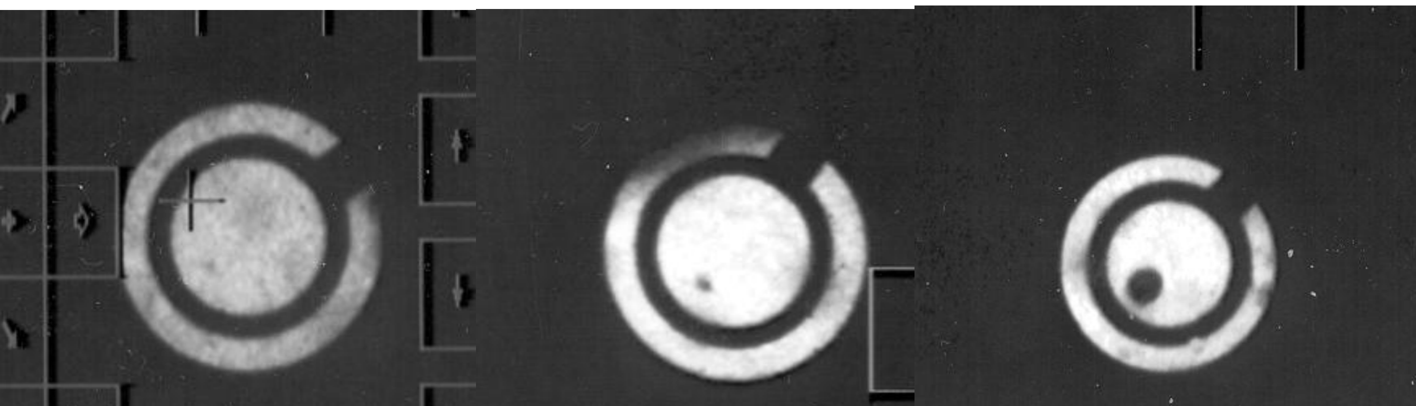
Degradation of a leakage path of a LED



OBIRCH RBL-localisation (reverse direction)

Emitted light power reduction of LEDs with different RBL





Forward operation: missing light emiss-ion in the leakage spot (dark spot). It increases and thus, the total emitted power decreases

ESD on LEDs doesn‘t stop function, but reduces their lifetime!

Obstructions in the process sequence by electrostatic charging in insertion machines

When pulling-off the deck tape slowly (here demonstrated manually to have a better access for photography) non-antistatic material will cause electro-static charging. The resulting electrostatic adhesion fixes small devices partially at the deck tape, thus significantly disrupting the mounting- or placement process, here demonstrated at the example of small SMD-LEDs.

What is ESDFOS ?

ESD From Outside-To-Surface

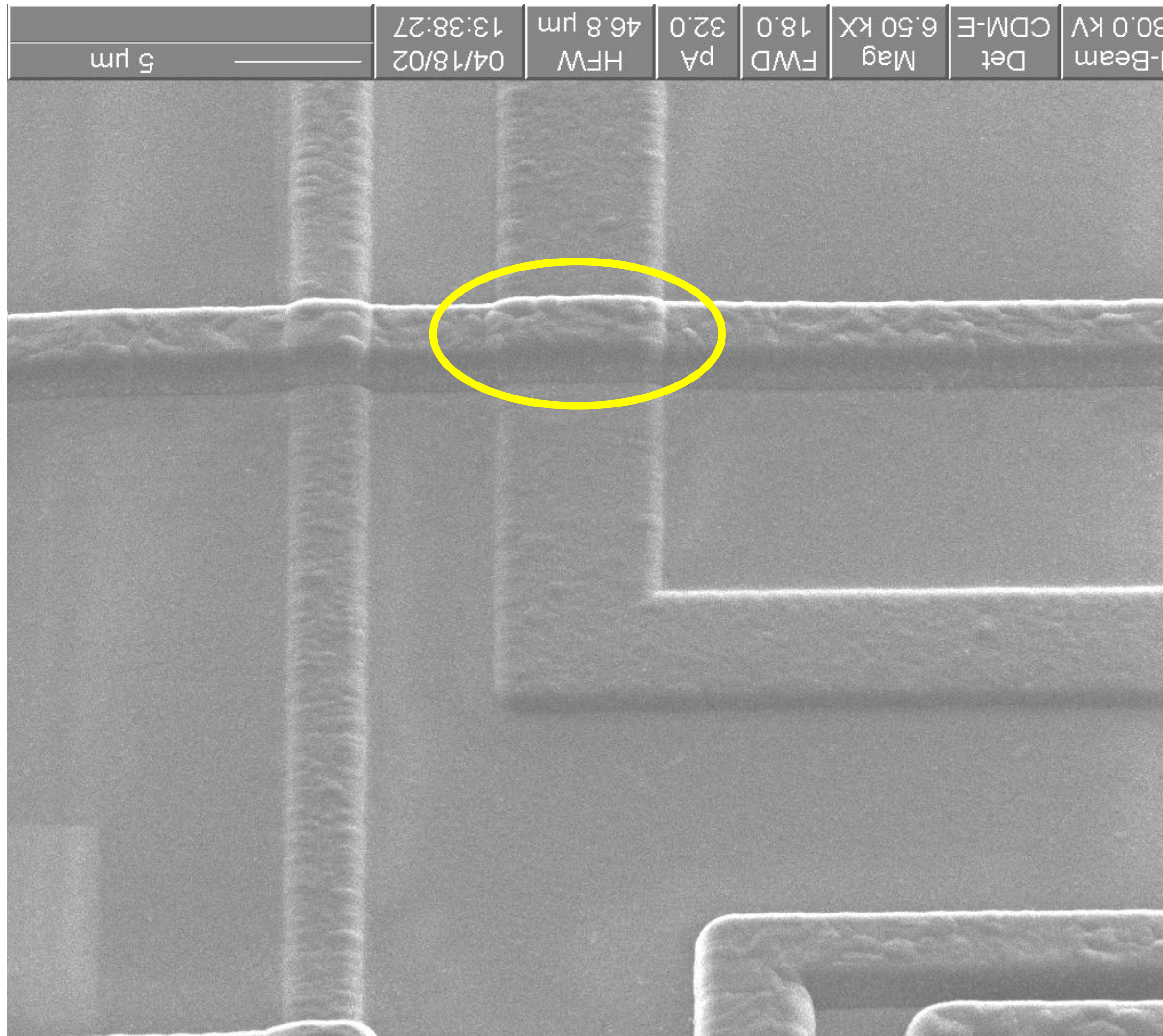
- ESD impact directly into the chip surface (cracking the passivation), bypassing ESD-protective circuitry
- normally caused by assembly processes between wafer final test and device packaging/ chip on board
- not applicable to common ESD tests like CDM, HBM, MM, (VF)TLP

Optical microscope

Found by random optical inspection !!

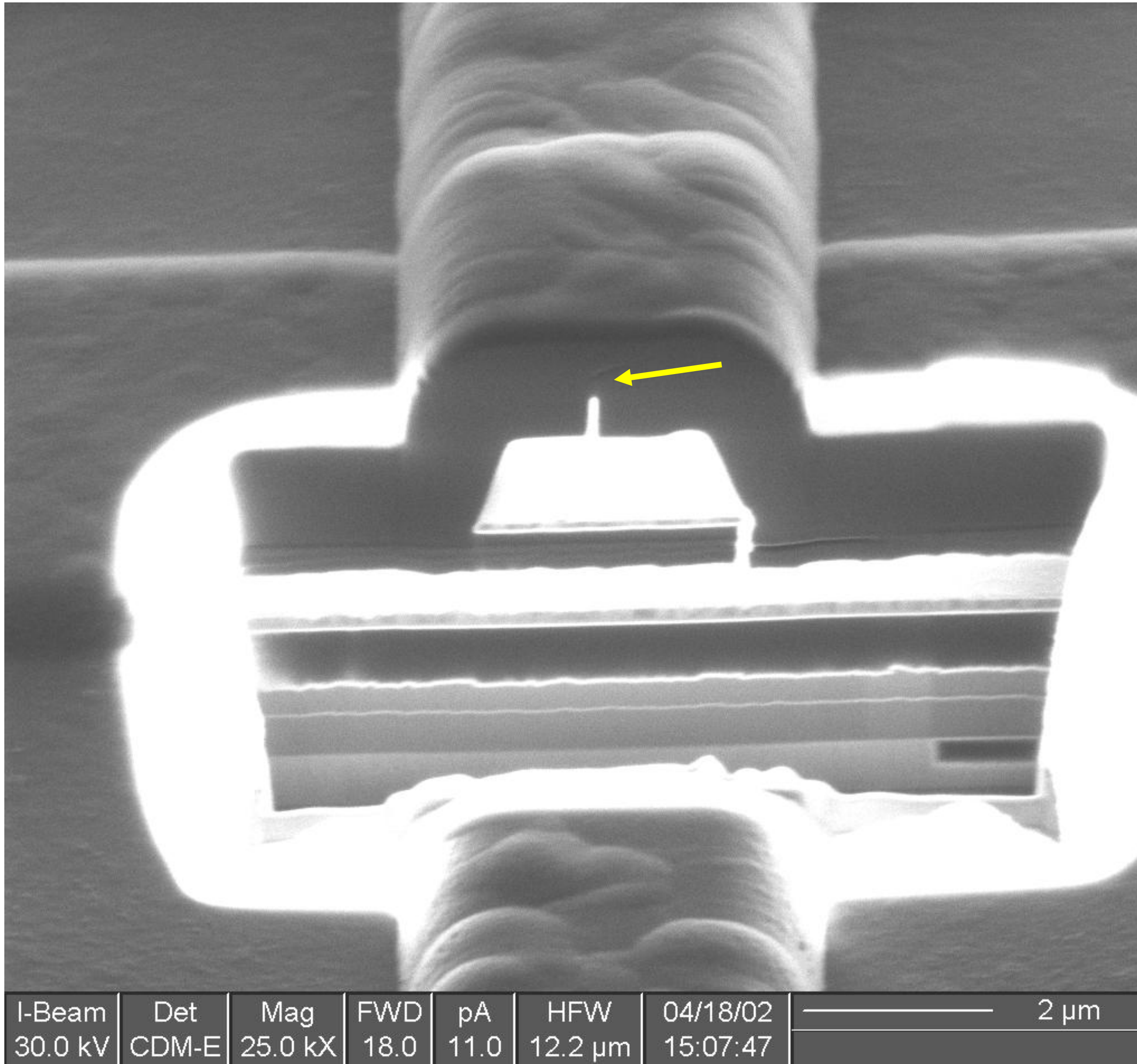
?

Nearly invisible ESDFOS



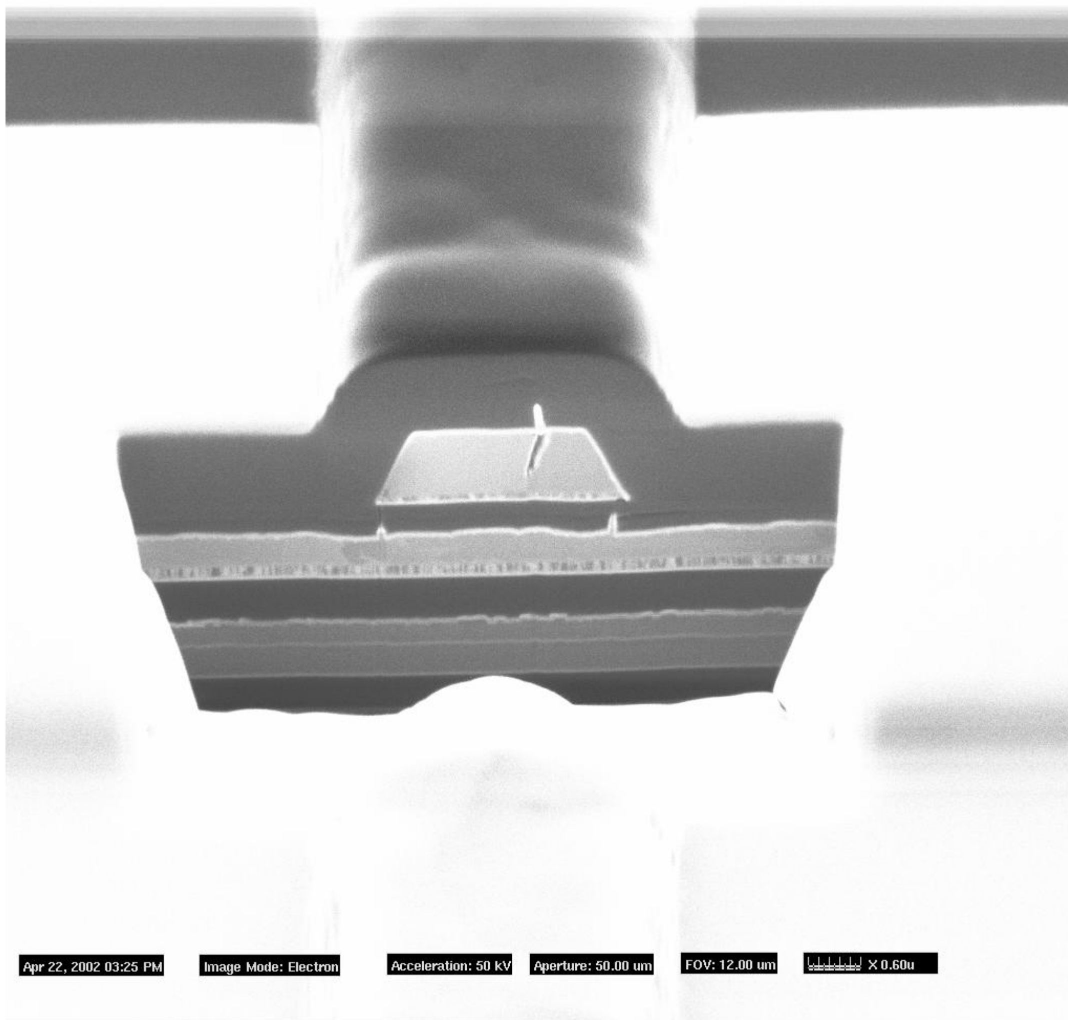
A small crack, hardly visibe in an optical microscope, nearly invisible by FIB or SEM, indicates the impact

FIB-Cross Section of this ESDFOS



FIB CS: M1-M2 filament interconnect. Small needle peaks (arrow) indicate the ESD-related cause of the problem

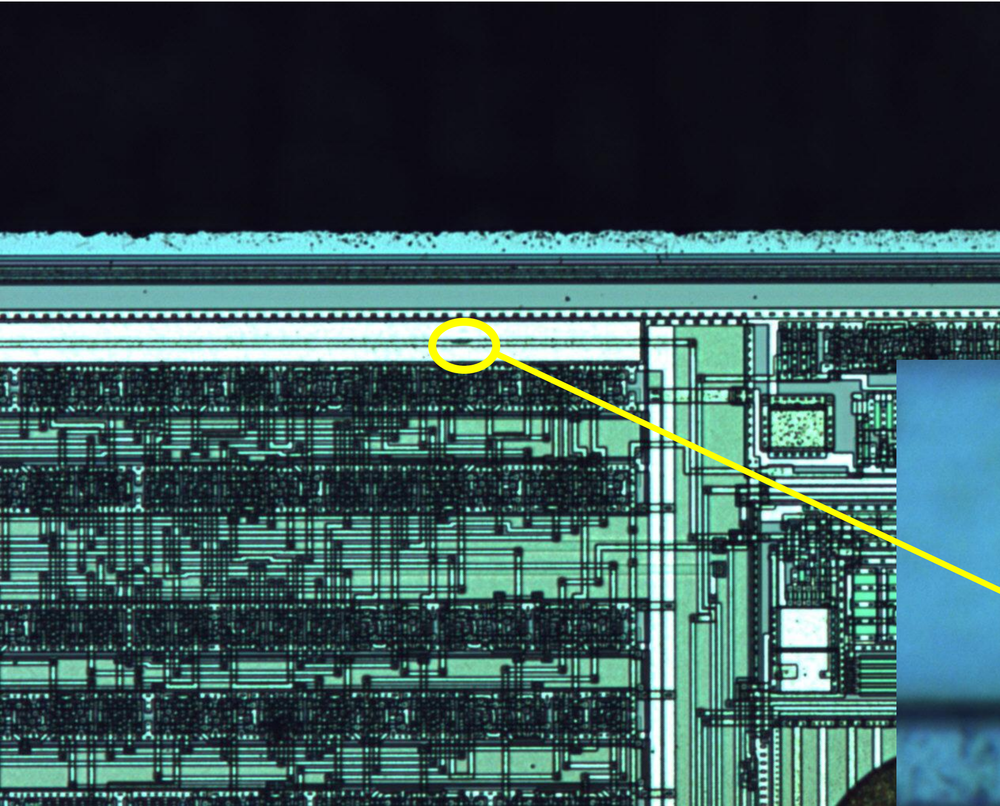
Reliability: Latent ESDFOS

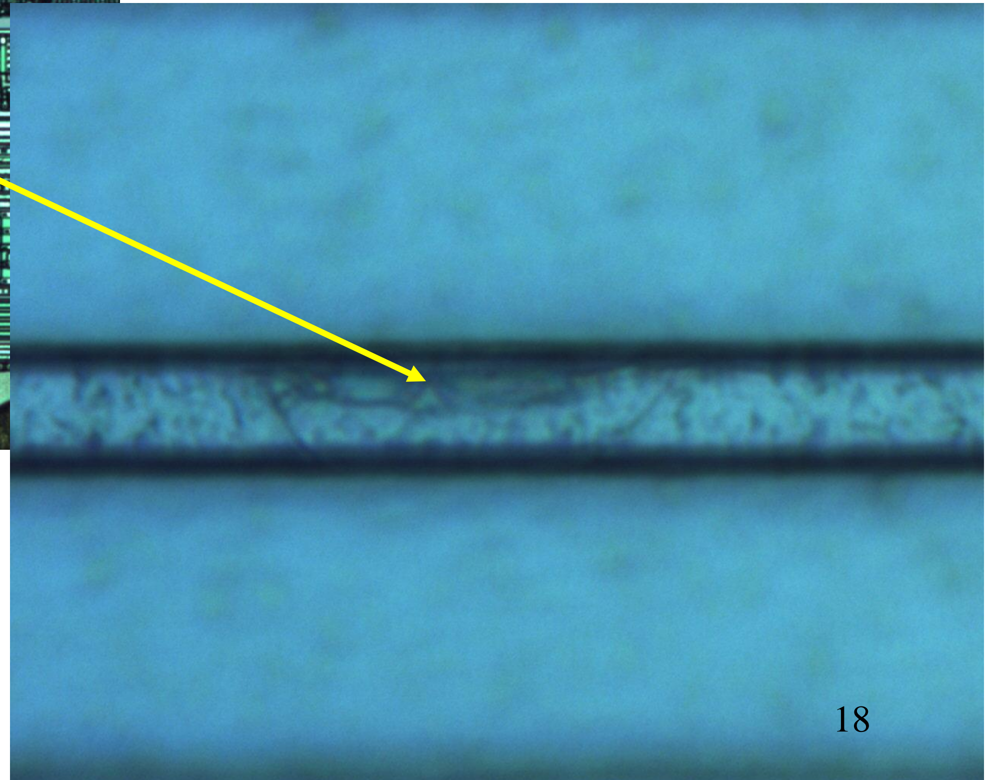


Reference device, elektrically good, next device on tape, neighboured to a bad one. „Blind“ FIB-cut at the same position: Latent ESDFOS failure

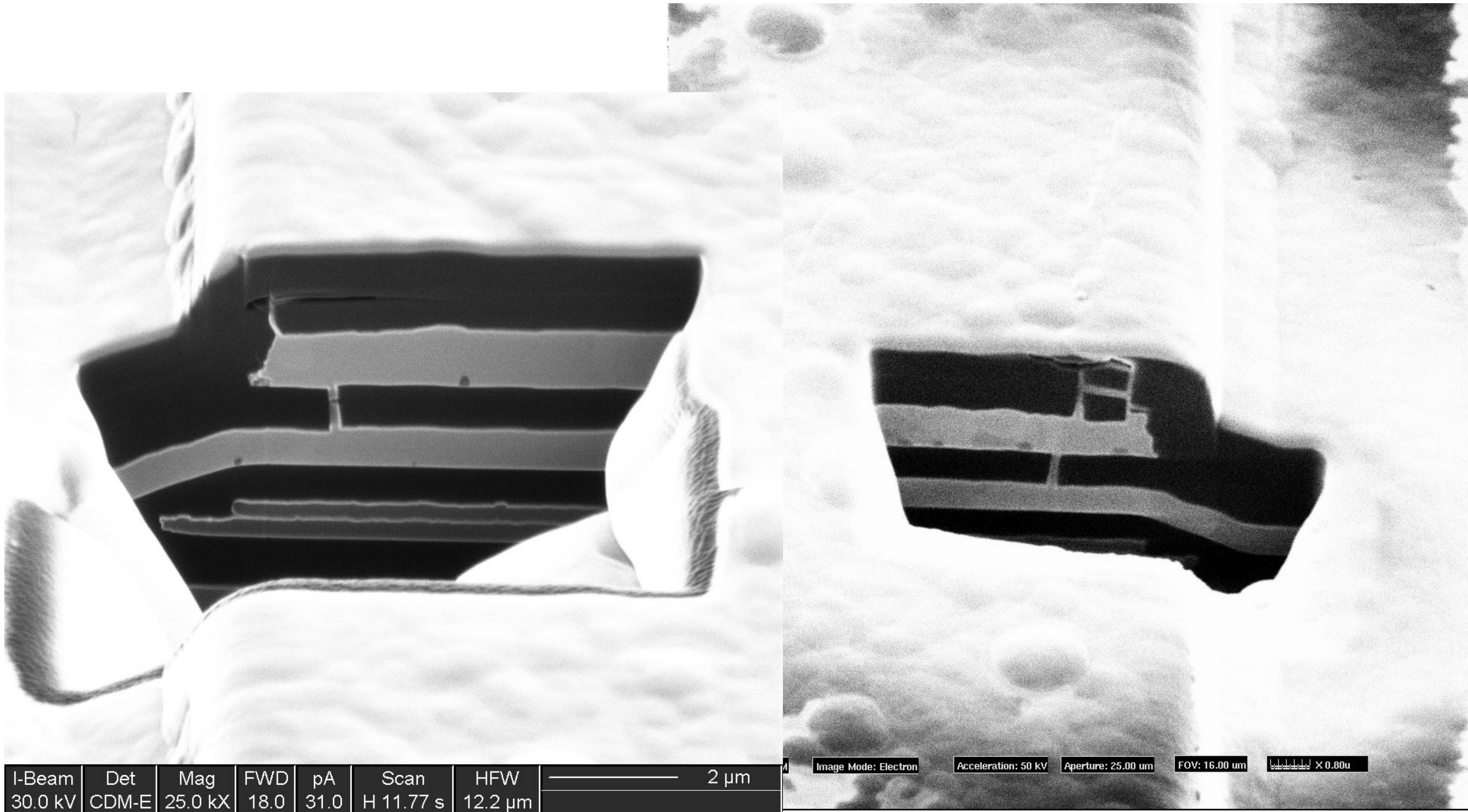
Chip border ESDFOS

ESDFOS main root causes: Frontside wafer detaping, wafer dicing, wafer separation after laser dicing, pick&place, framed-wafer lifting from chuck, then loading into cassettes

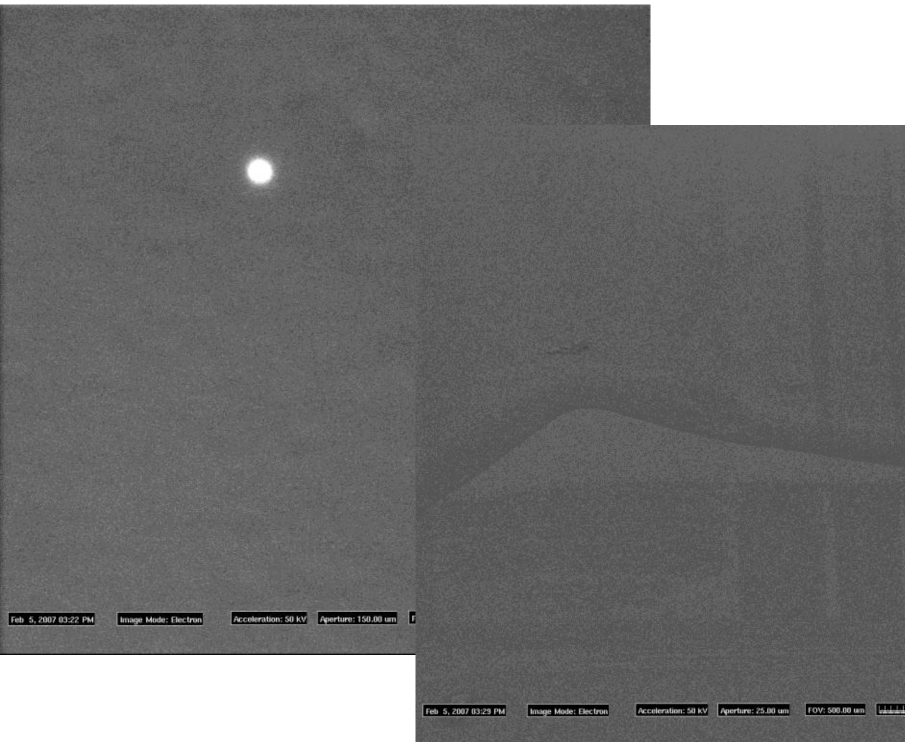


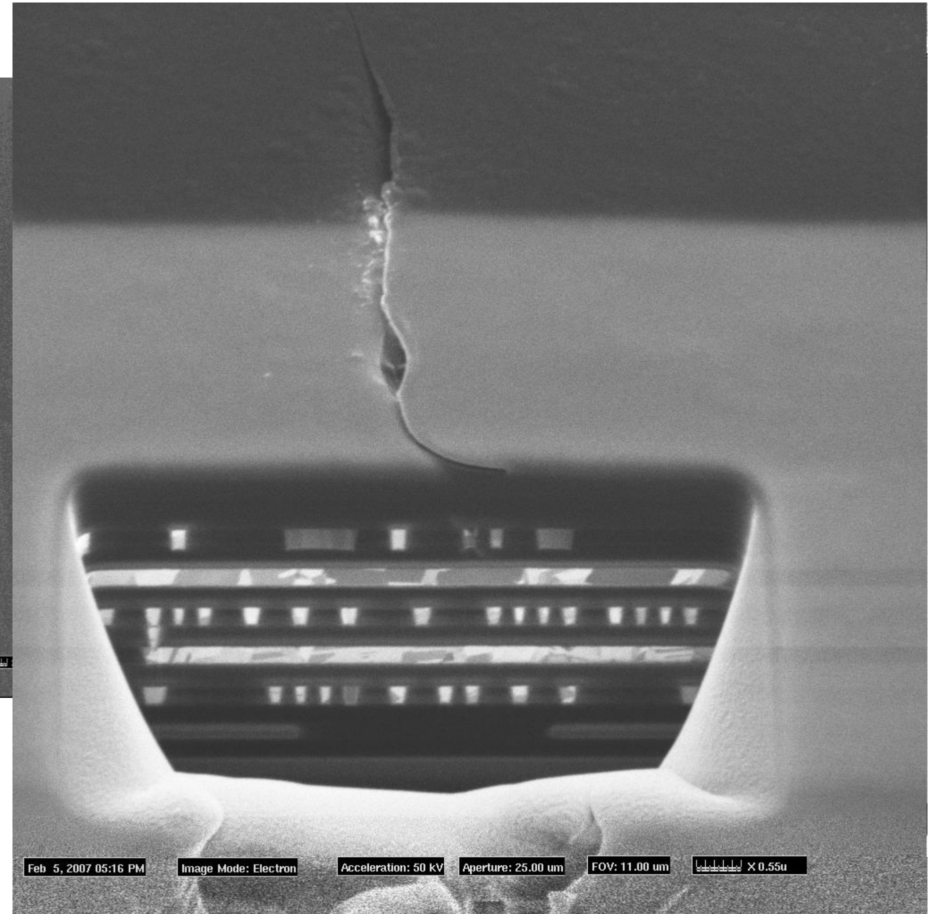


Chip border ESDFOS



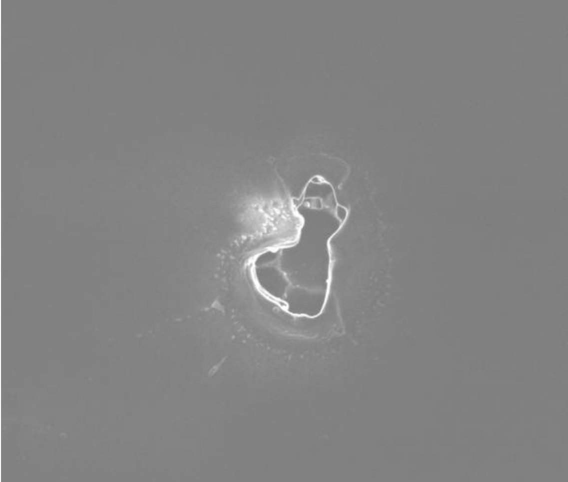
ESDFOS in planarized Cu-metal technologies: Low degree of severity

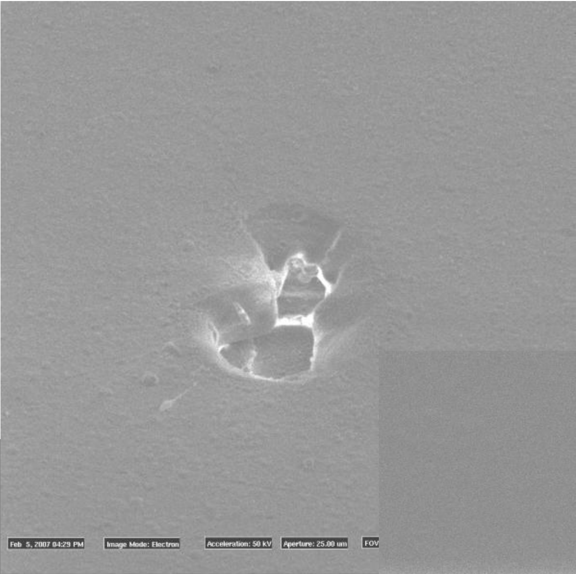


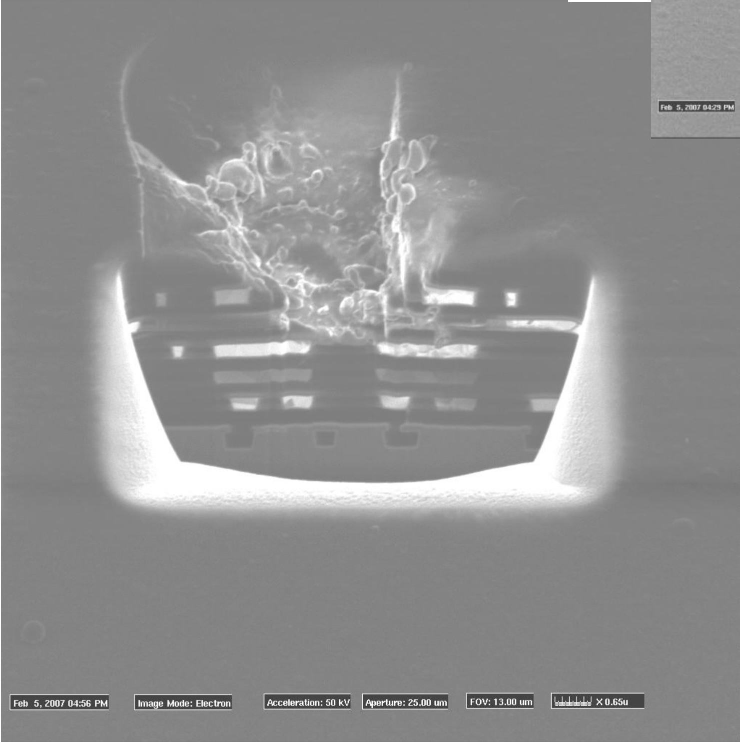


very small cracks, strong horizontally oriented, partially without functional damage

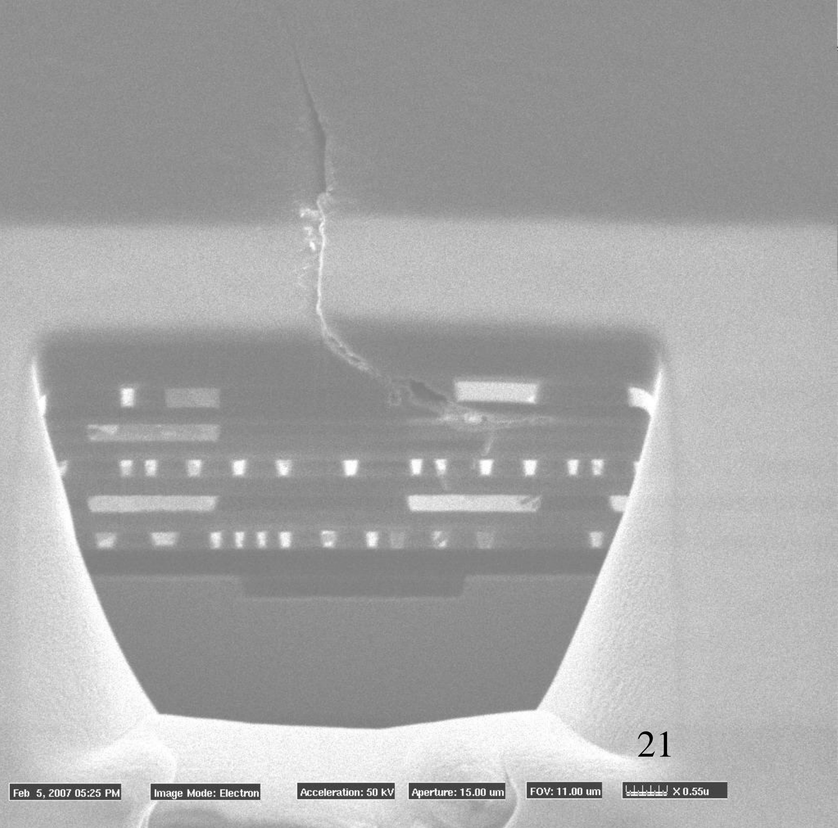
Medium degree of severity



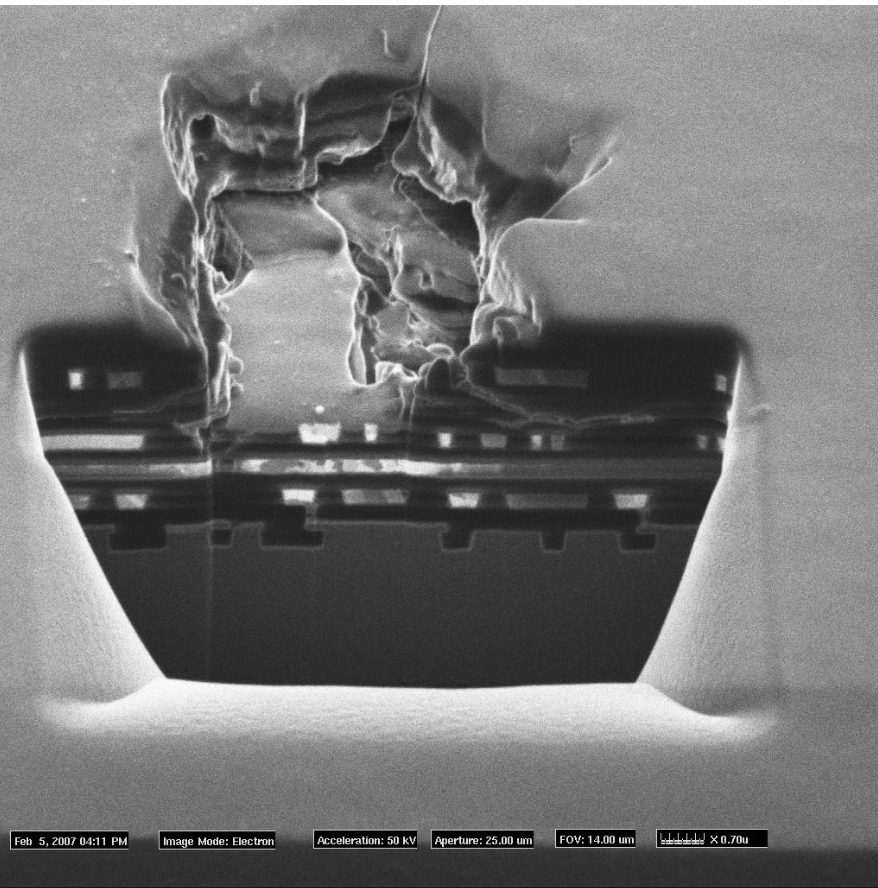


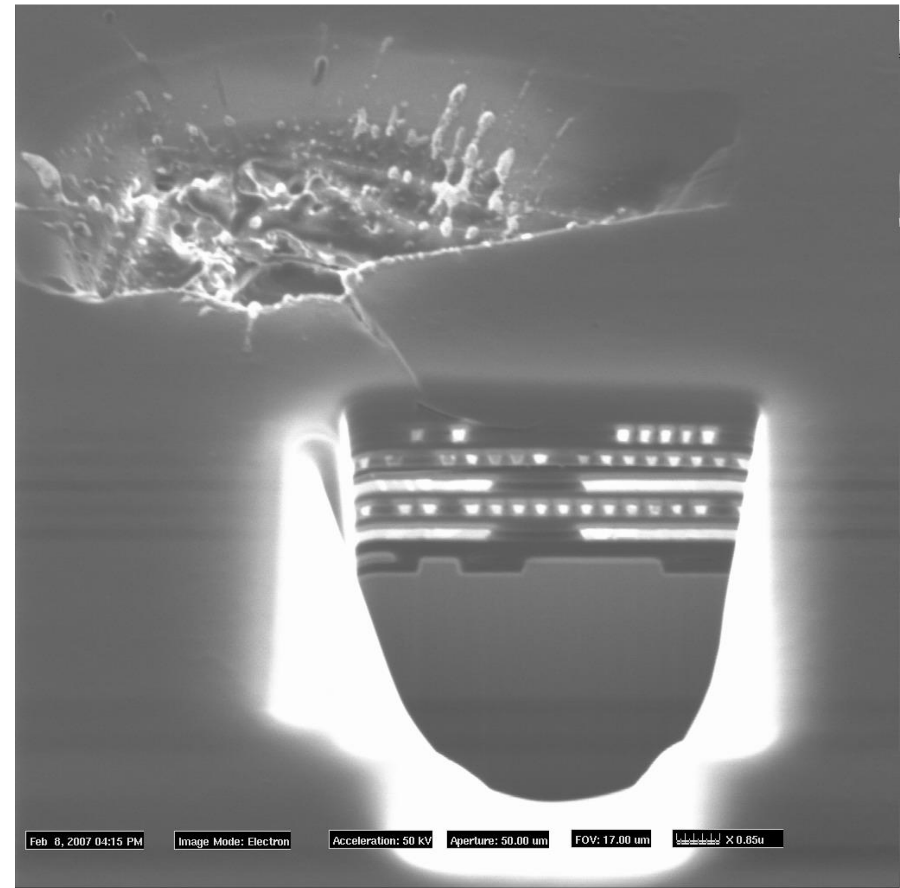


the top1-2 metal layers are damaged



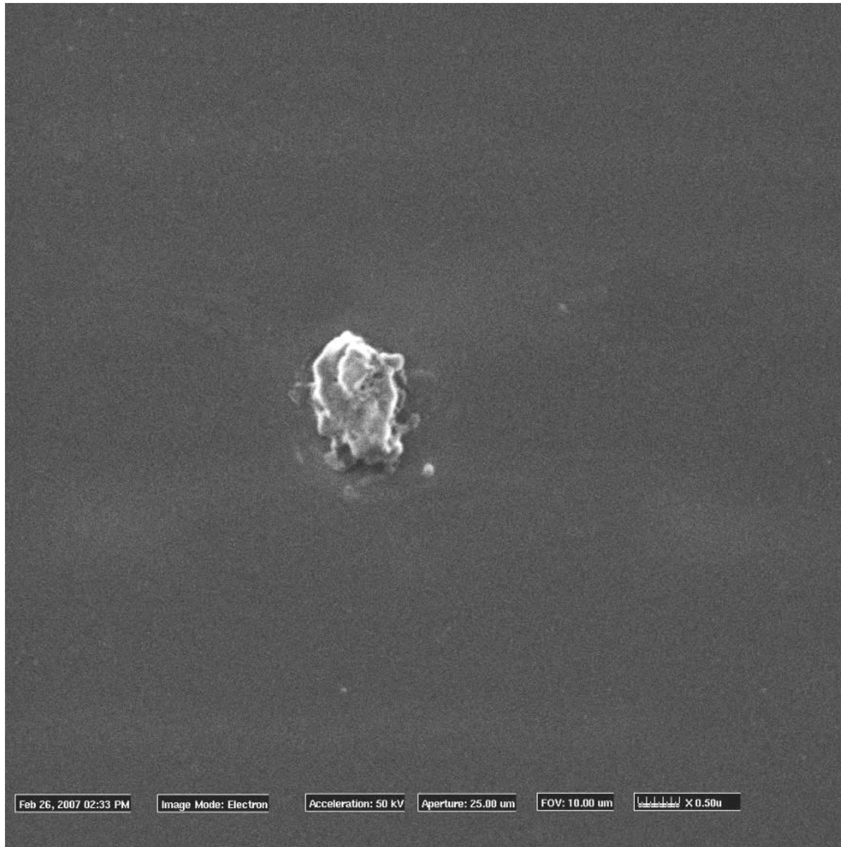
Severe degree of damage

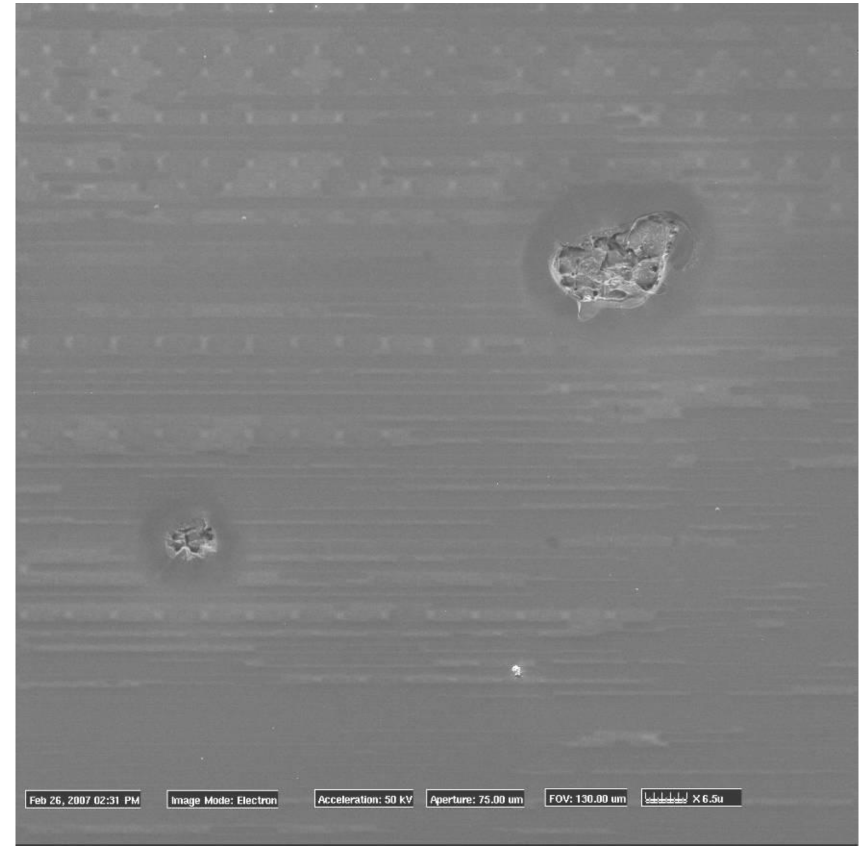




Those damages involve deeper metal layers, too; sometimes "explosion-like" signature with strong horizontal components

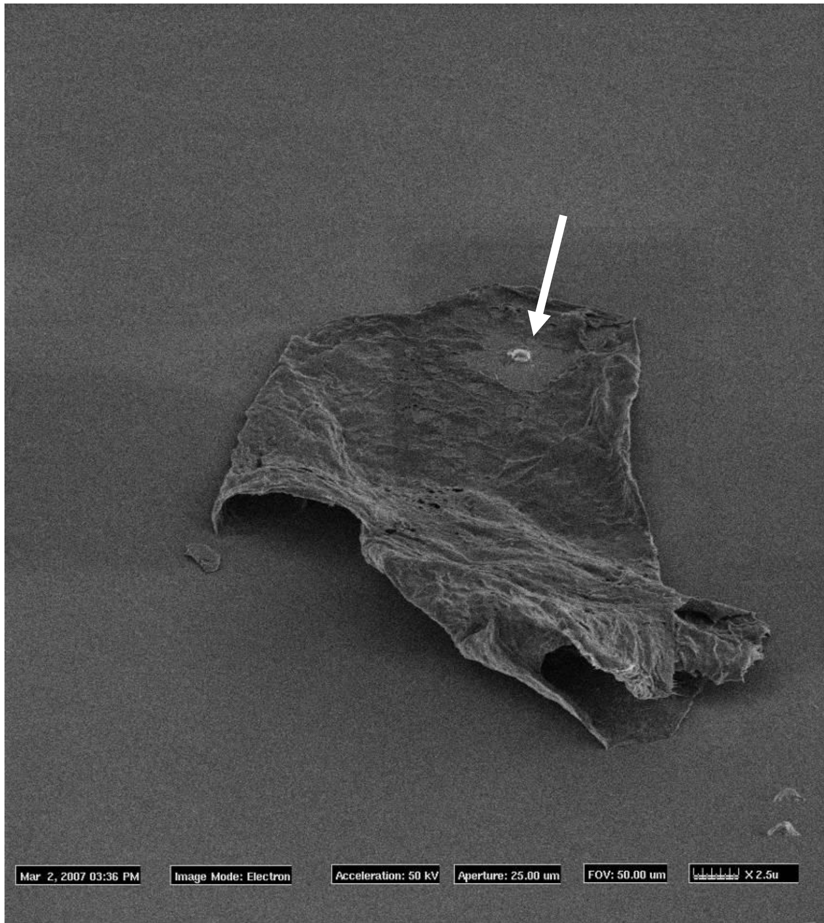
Particle embedding





Since particles are elevated on planar passivations, they serve as a priorised target point for ESDFOS. ESDFOS fixes them by point-welding and, thus, mask the real ESDFOS impact.

Fixing a pancake particle by ESDFOS welding



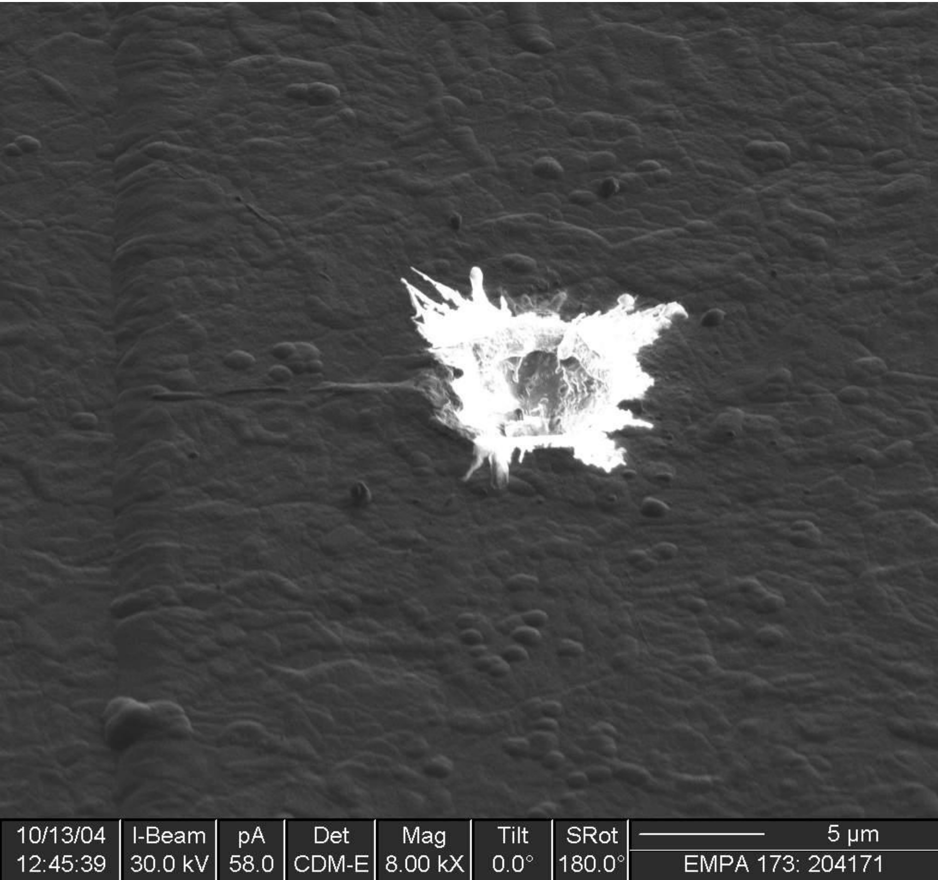
Nobody would assume ESDFOS when finding such a particle…

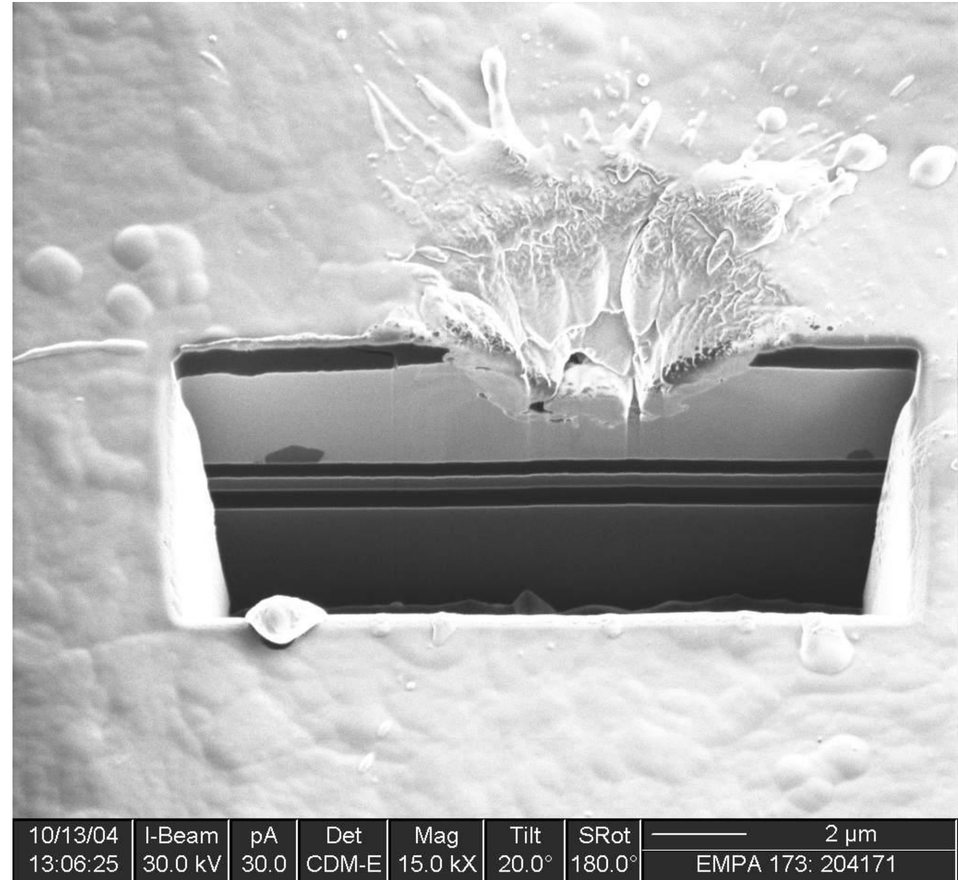
...however, a FIB-cross section proves exactly this (180° rotated, cross sect-ion through the ESDFOS impact hole

- Thick passivation:the amount of energy consumed in the air (ionisation, acoustic, light) shifts itself towards the device.
- Thus ESDFOS damage in Cu appears more severe but less frequent
- The risk of mixing-up with mechanical damage is huge, even for experts!

ESDFOS in IGBT-chip

Power devices are self protected to a certain degree by their high capacitance

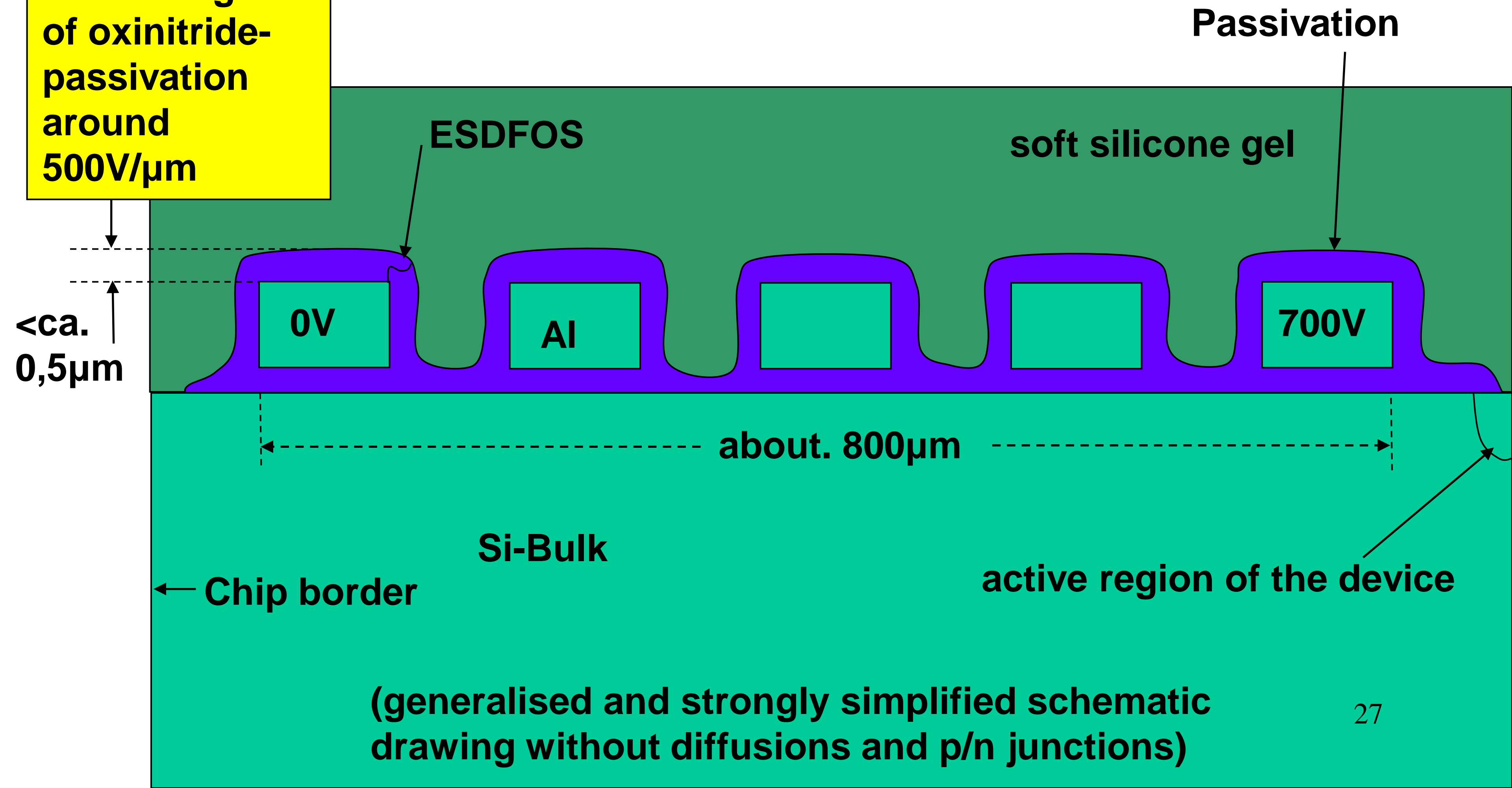




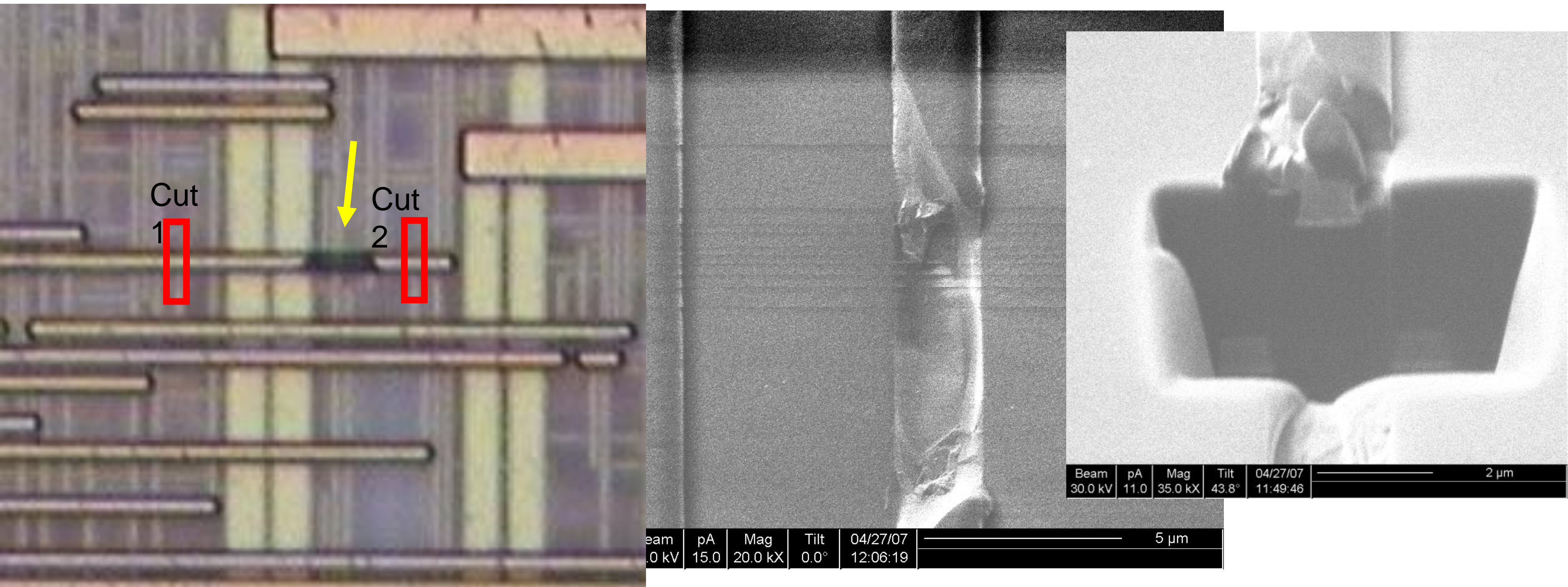
ESDFOS impact in a *passivated region*. The impact melts material of the volume and throws it off, like a vulcano. Both impact types (metal surface and passivated) don't cause direct structural damage like on microelectronic devices. Gate ox breakdown and/ or p/n leakage may sometimes appear on distant locations instead.

Cross section of a field plate ring border

If humidity-induced creeping current occurs at the bottom side of the soft silicone gel layer, a < 0,5µm thick passivation cannot prevent a field-induced breakdown in case of a locally ESDFOS-pre-damaged passivation.

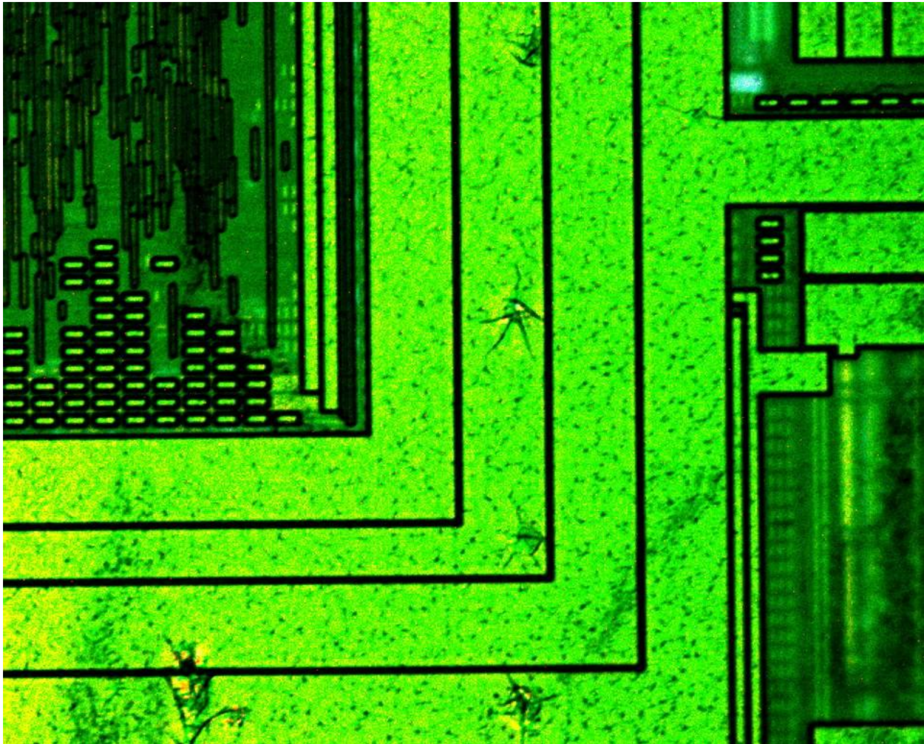


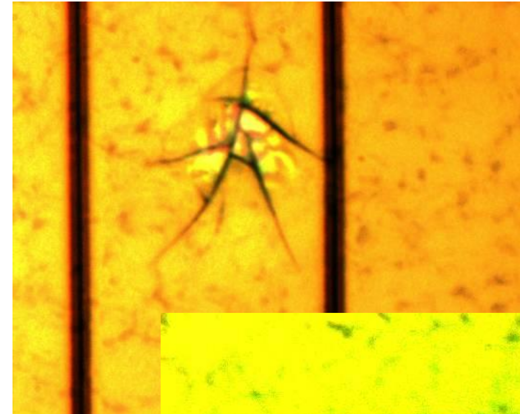
Mechanical metal spalling by ultrasonic force and/ or frontside detaping

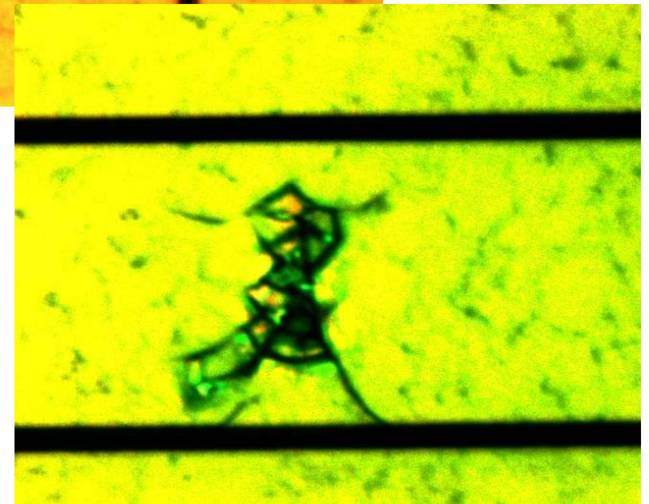


Cavities induced by an„unintended ultrasonic cleaning“ during wafer sawing can generate ESDFOS-similar mechanical damage. Verification needs FIB-cross-sectioning, especially interlevel dielectric shorts and needle-like-aluminum-peaks are missing in such cases.

Ultrasonic Cleaning Induced Defects



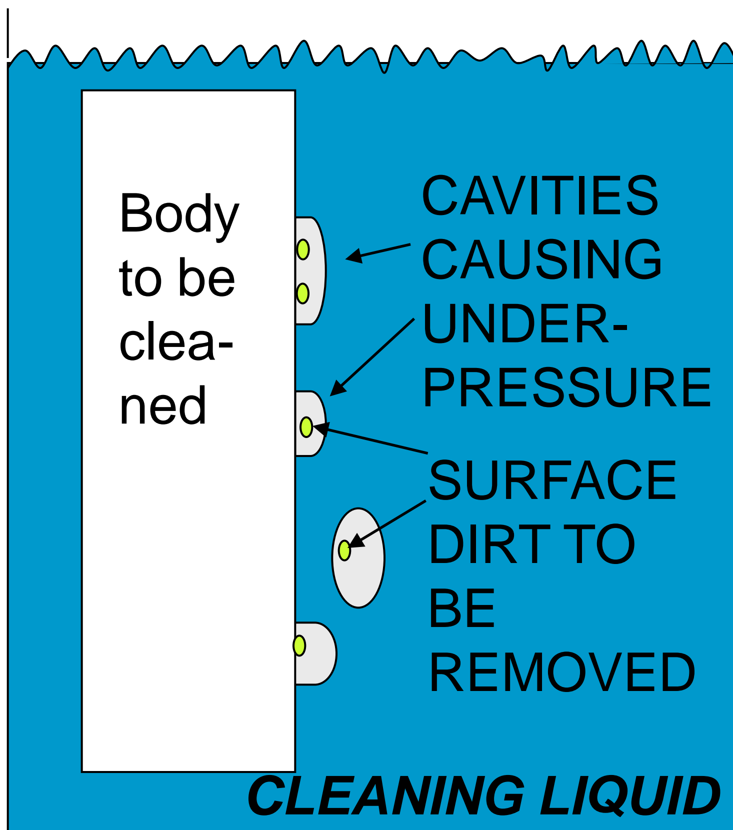


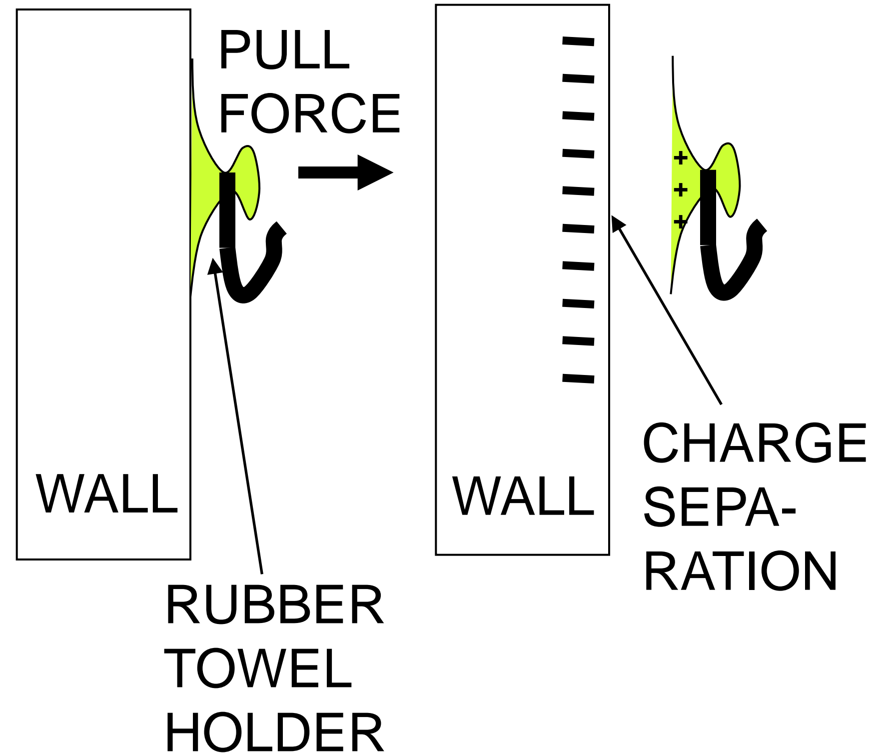


Reproducible defects, originating from an ultrasonic cleaning bath with some days old DI-water. After water renewal, the defects could not be reproduced anymore

Jacob, Rothkirch, Best Paper ESREF 2008

Ultrasonic Cleaning Effects



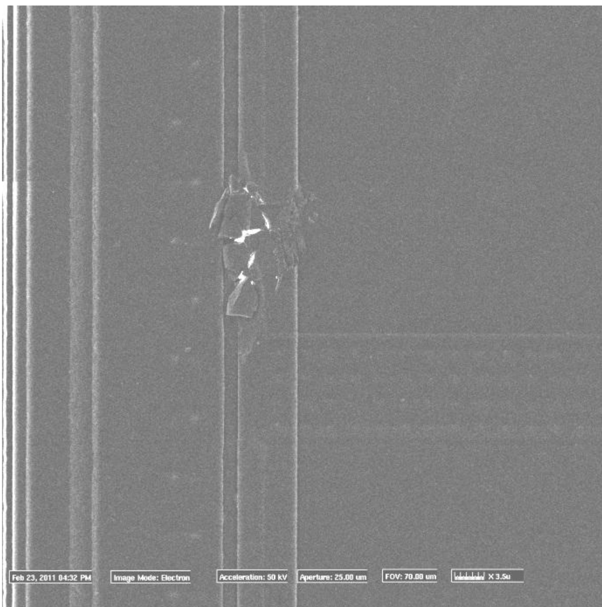


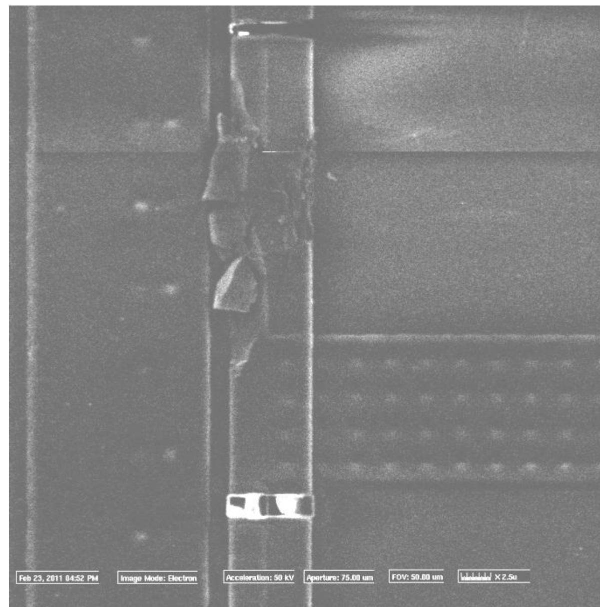
„Vacuum“ cavities clean the object (left) Under certain circum-stances, ultrasonic cleaning may generate charging, too (right)

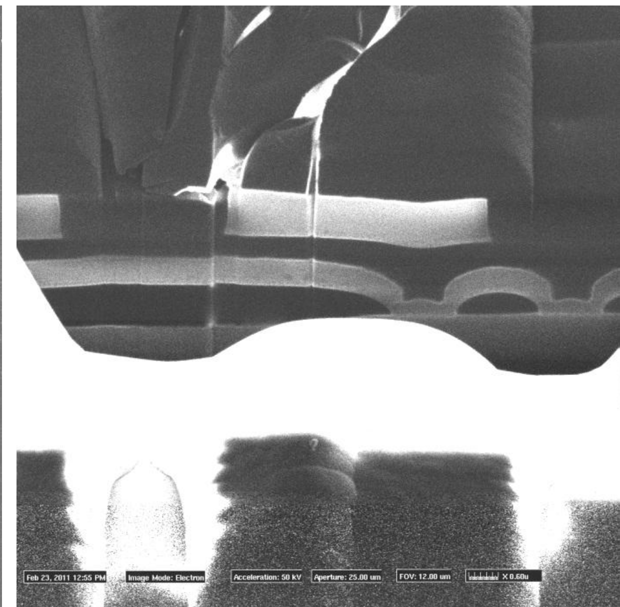
The wafer sawing process generates ultrasonic frequencies

Jacob, Rothkirch, Best Paper ESREF 2008

Pick&Place may cause similar non-ESDFOS damages, too !

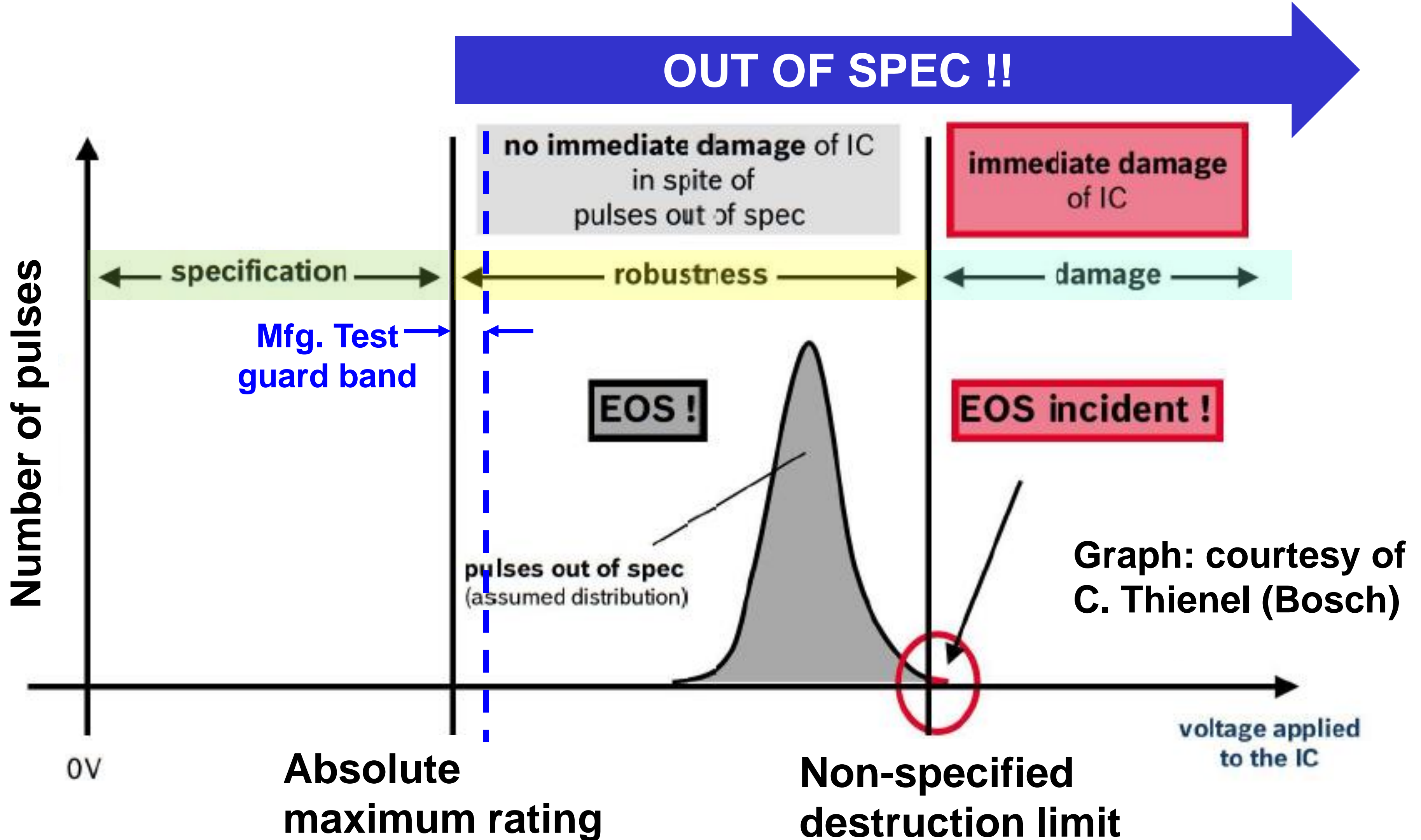






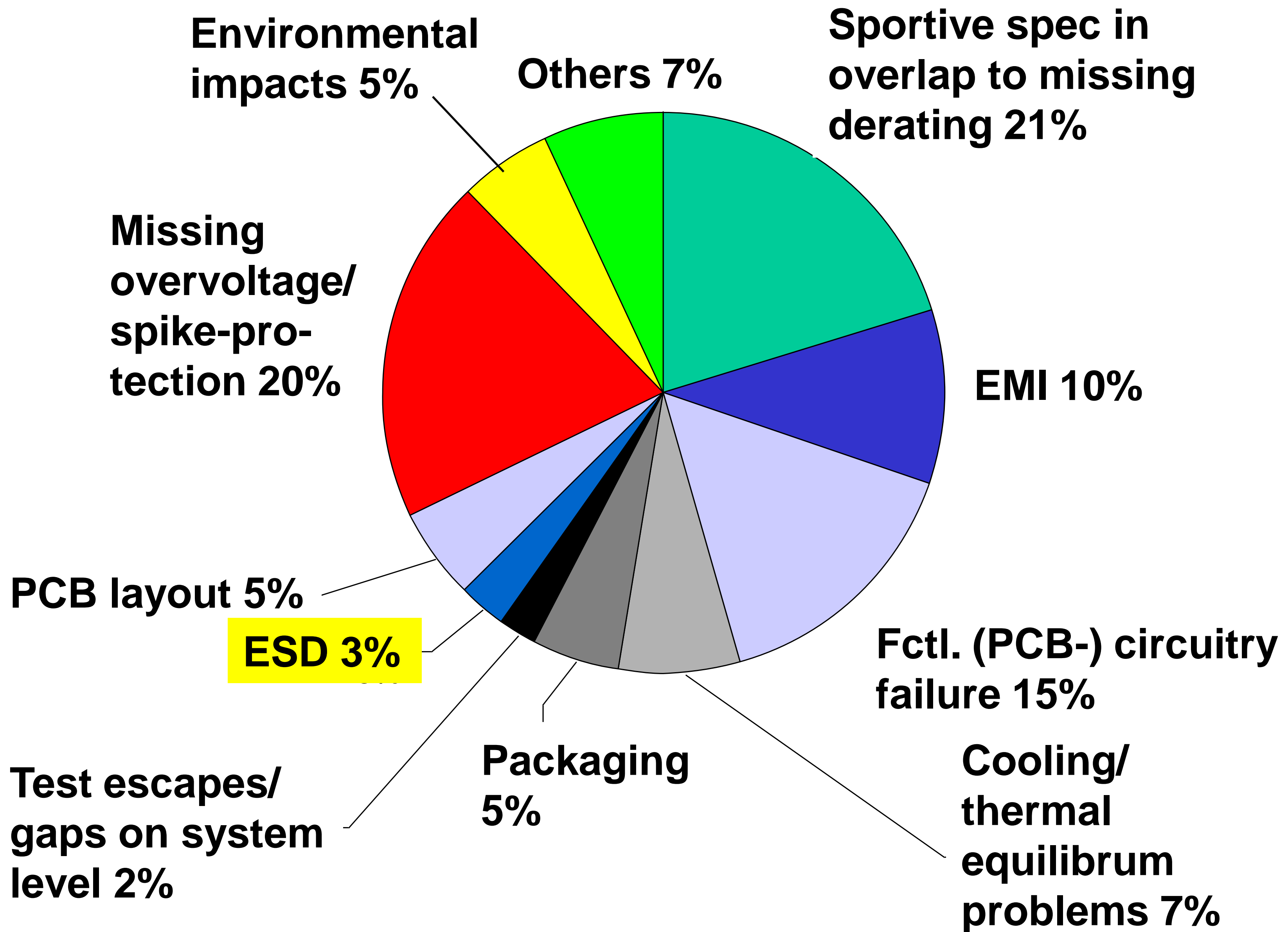
ESDFOS-like looking damage, caused by a small Si-particle adheasing at the rubber-made picker head, which damaged the passivation. A passive potential-contrast examination (center) shows that the top metal is not electrically connected to the metal underneath, as it would be significant for ESDFOS

ESD/ EOS: Where starts EOS?



EOS starts beyond specifications!

Important device failure root causes, originally rated as „EOS“



Conclusion

- ESD damage is possible through the pins but also through the passivation as long as we deal with wafers and bare dies (ESDFOS)
- ESDFOS can be hidden under welded particles
- ESDFOS-similar damage may be caused by thermomechanical effects and by ultrasonic cleaning
- ESD (pad)-similar damage may be generated by EOS, mainly by non-protected inductive voltage response and pulsed EMI
- ESDFOS damage on Cu- and Al-metallized devices show-up very different
- Sound F/A experience needed to distinguish between ESDFOS and ESDFOS-similar, but thermomechanical or ultrasonic-related damage or EOS-related failures
- ESD models show discharge mechanisms but cannot cover the wide variety of real-world-ESD.