ESD LAYOUT CHECK TOOL: APPLICATION TO RF IC DESIGNS

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Outline

- Introduction
- IC Level ESD
- HBM layout Simulations
- Predictive CDM Simulations
- Conclusions

Introduction

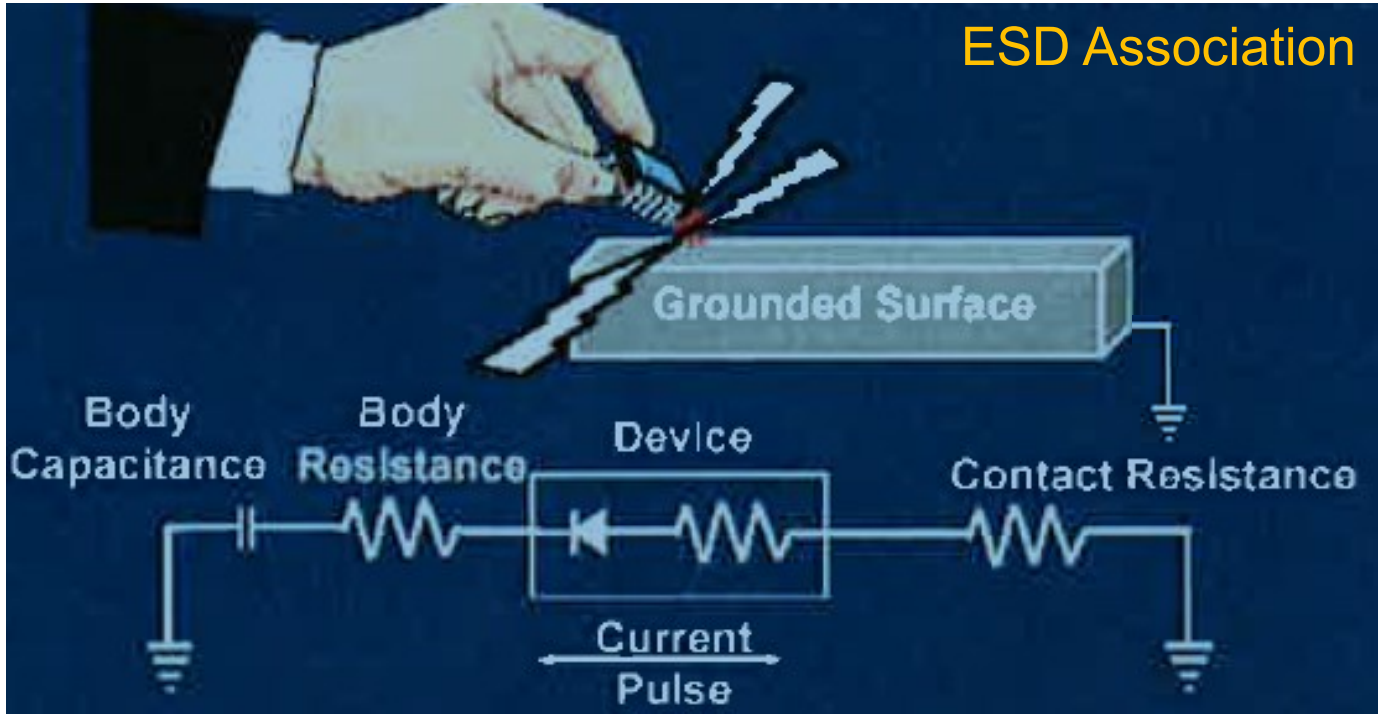
- Context:
  - Rapidly increasing RF Complexity of RF BiCMOS IC designs
  - Key Mobile, Internet Everywhere and Car Radio applications
- Extreme RF performance vs. NXP IC's ESD reliability requirements:
  - Big challenge to achieve first time right silicon for both
  - ESD layout check tools are essential to verify proper layout implementation
- ESD Layout Check tools are applied to RF IC designs in NXP propriety RF BiCMOS technology

IC Level ESD

- IC's can be exposed to ESD during assembly
- ESD on-chip protection is used to protect IC during manufacturing
- Qualification of IC by (JEDEC) standards:
  - Human Body Model (HBM)
  - Charged Device Model (CDM)
- Stresses are applied to all the pins of the IC

Courtesy of Theo Smedes

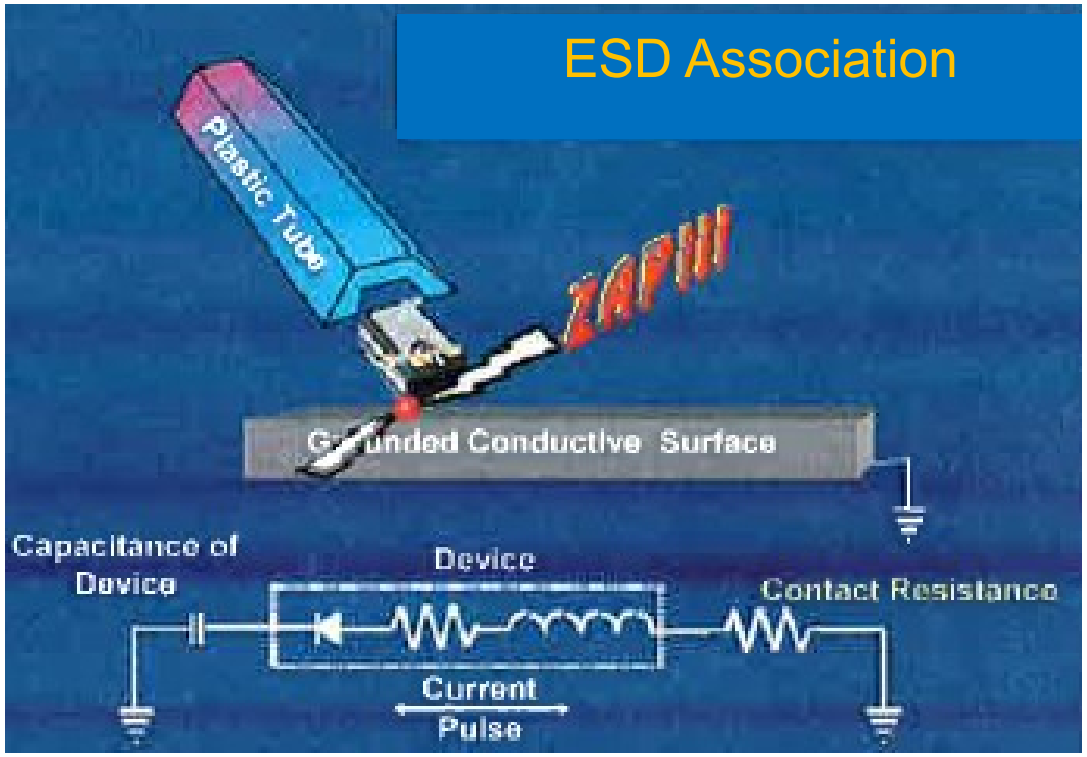
IC Level ESD: Human Body Model (HBM)



HBM Characteristics	
Qualification Level	2kV
Pulse Width	~150ns
Rise Time	2-10ns
Peak Current	1.33A

- HBM: Where a charged human gets discharged by making contact to exposed IC pins

IC Level ESD: Charged Device Model (CDM)



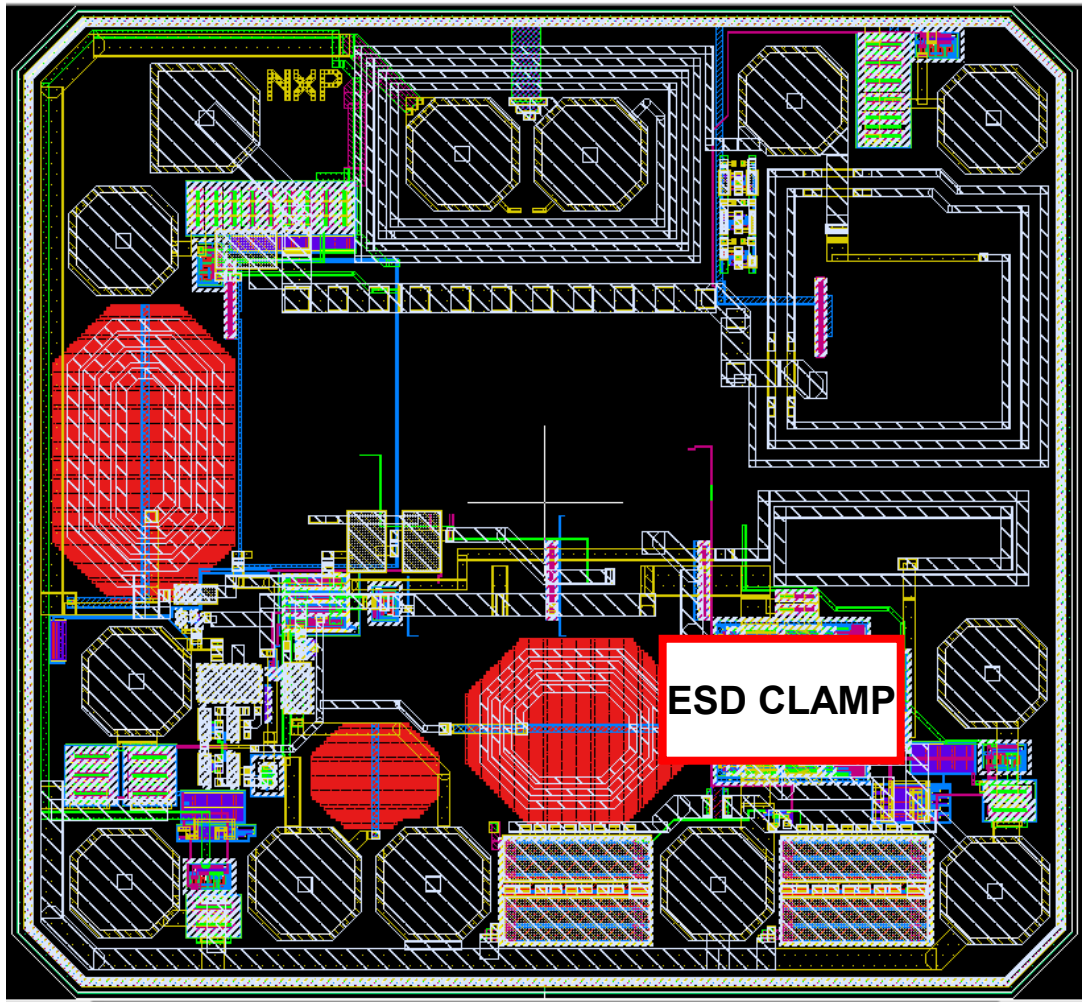
CDM Characteristics	
Qualification Level	500V
Pulse Width	~1.5ns
Rise Time	100-300ps
Peak Current*	1-15A

** IC package dependent*

- CDM: IC packages that acquire charge can discharge to ground through their pins

HBM LAYOUT SIMULATIONS

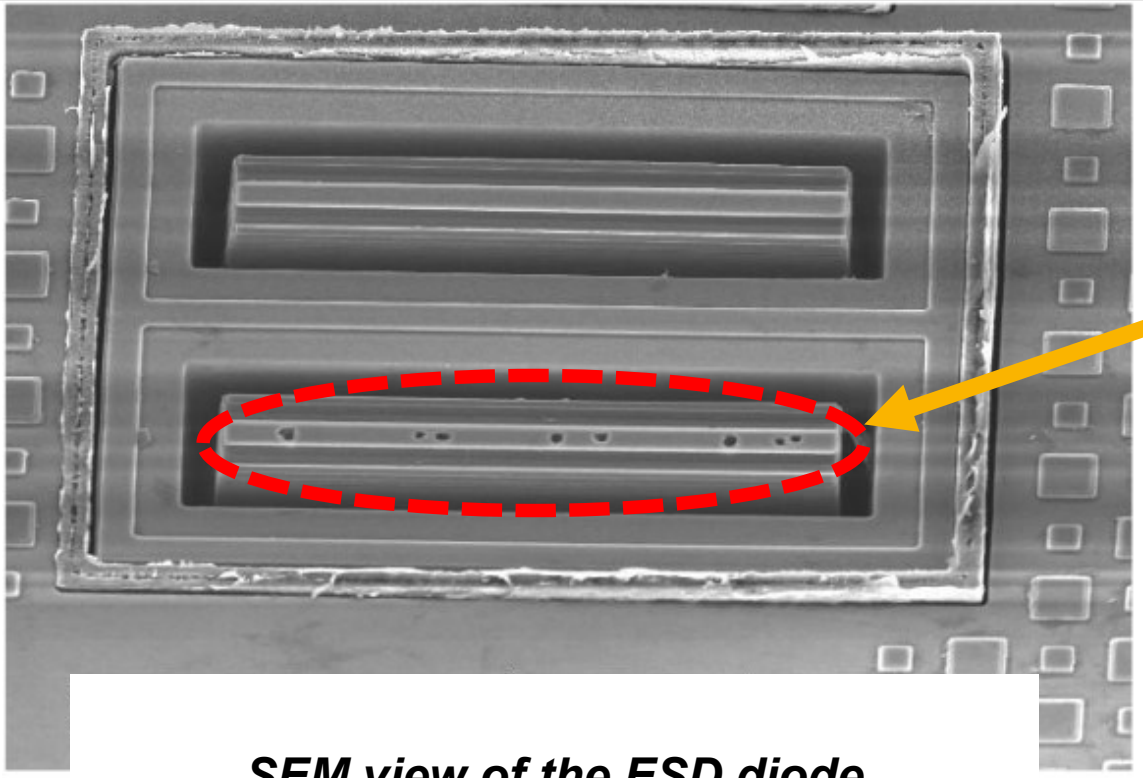
LNA Design



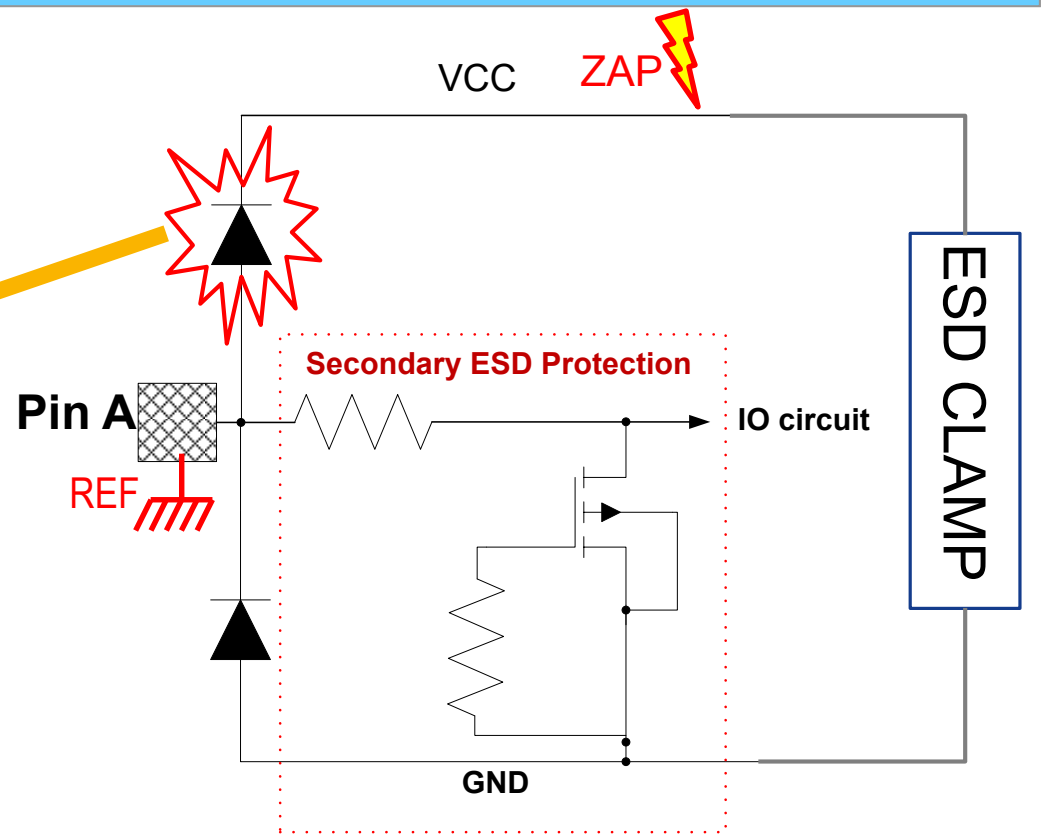
Backend view

- An integrated 800µm x 800µm low noise amplifier (LNA) and switch
- Processed in an NXP proprietary BiCMOS technology
- Integrated circuit used in RF modules for mobile applications

HBM Failure Mechanism

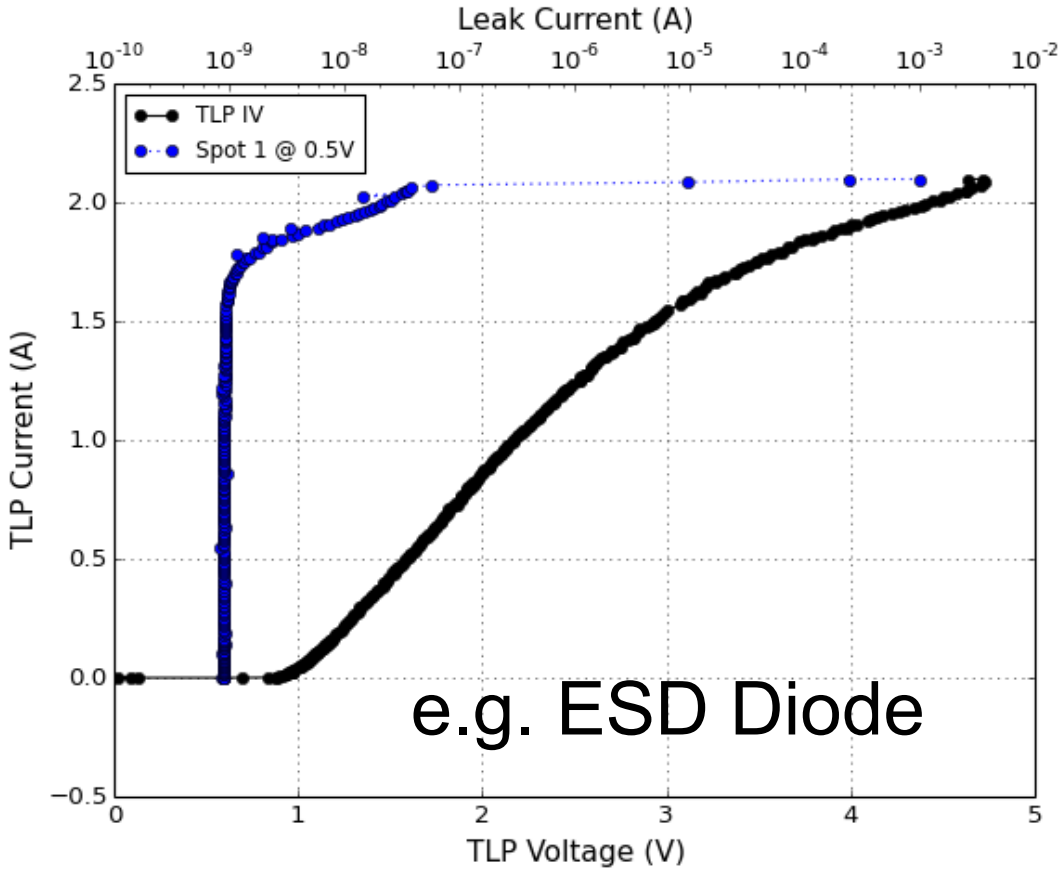


SEM view of the ESD diode



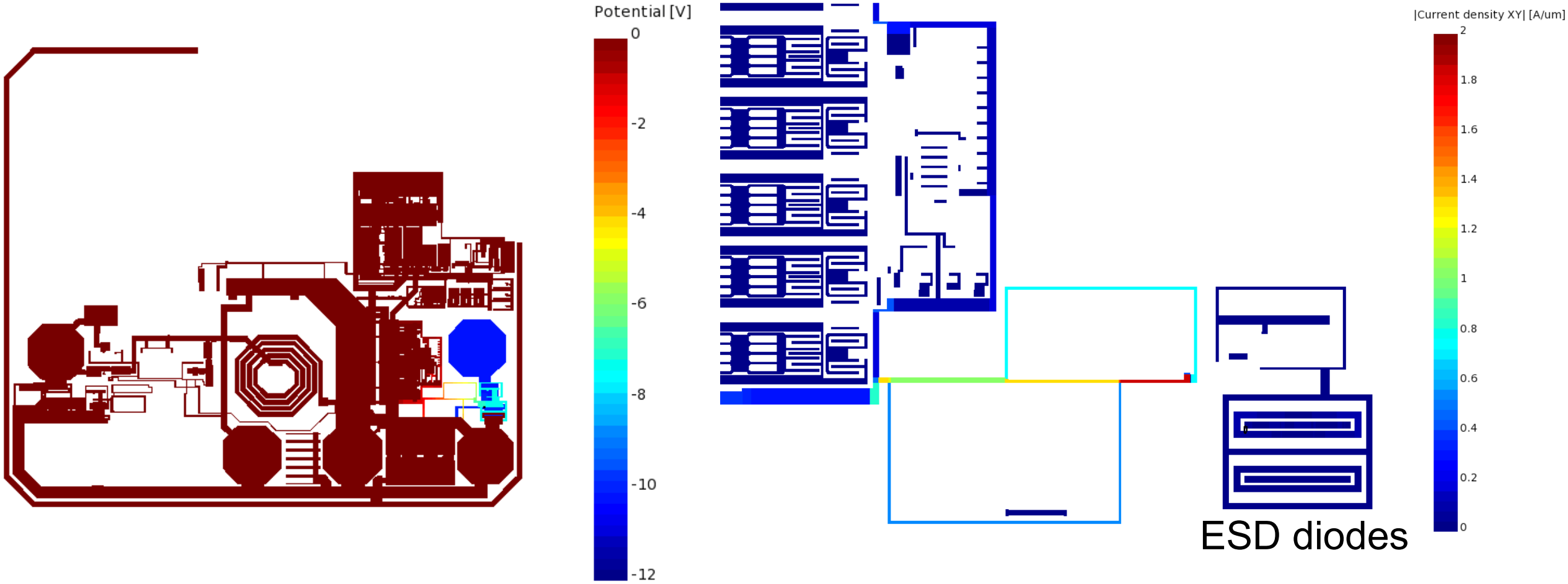
- During HBM zap, a high clamping voltage is built up across the ESD diode
- Leading to observed HBM failure: breakdown of the ESD diode

HBM Simulations: Input Data



- ESD Device (measured data)
- Design data (layout database)
- Technology Data (process layer map, ESD rule file)
- Execution Setup (description of the ESD tests of interest)

HBM Simulations: ESD Violations (1)



- High current density crowding is observed in the ESD diodes area

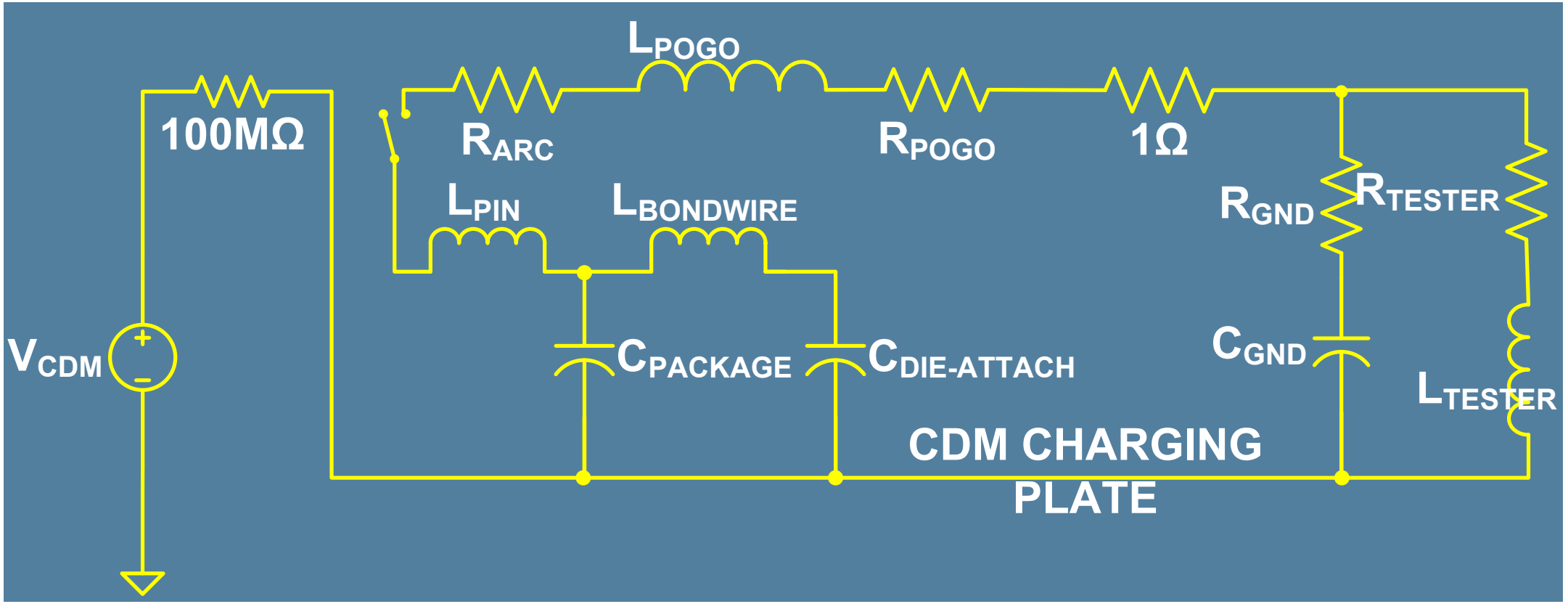
HBM Simulations: ESD Violations (2)

HBM Sim.	Zap name	Vclamp (V)	Ipeak (A)	Reff (Ω)	Stress,%
Fail	VCC vs. PinA	11.7	1.3	8.4	488%
Pass	VCC vs. PinA	8.6	1.3	4.2	0%

- High ESD current density (**488 % Stress !**) reported in the ESD diodes area by the HBM simulations
- **The observed HBM failure mechanism is identified by HBM simulations successfully !**
- A redesign metal fix was implemented and the HBM simulations reported NO violation (**0 % Stress !**)
- This was further confirmed with silicon results with HBM qualification pass.

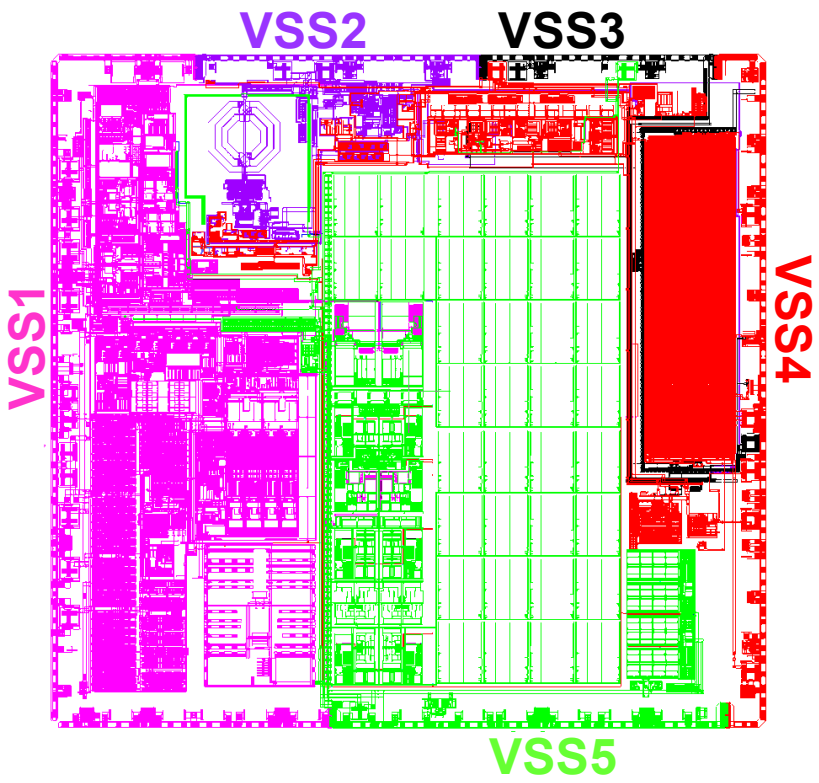
PREDICTIVE CDM SIMULATIONS

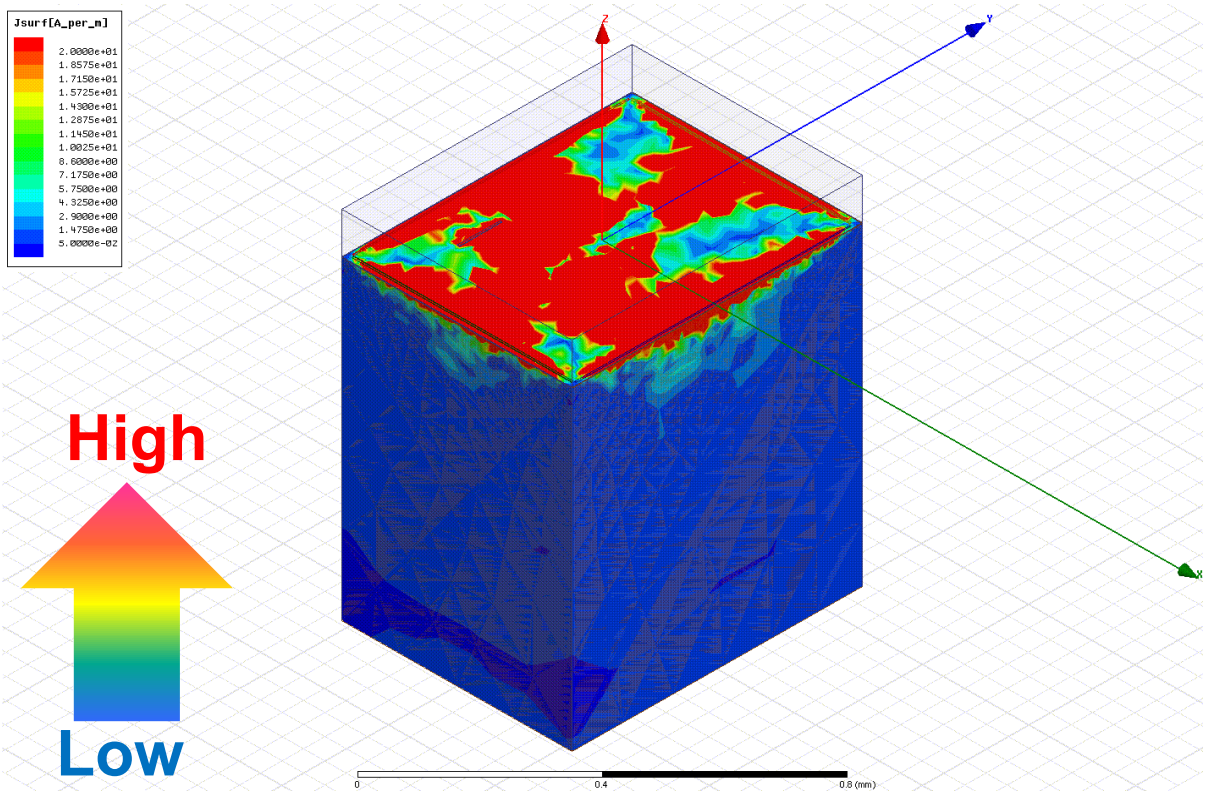
CDM Tester Model



- Model has been calibrated on Standard ESDA verification modules
- Simulated waveforms agreed with measured current discharges

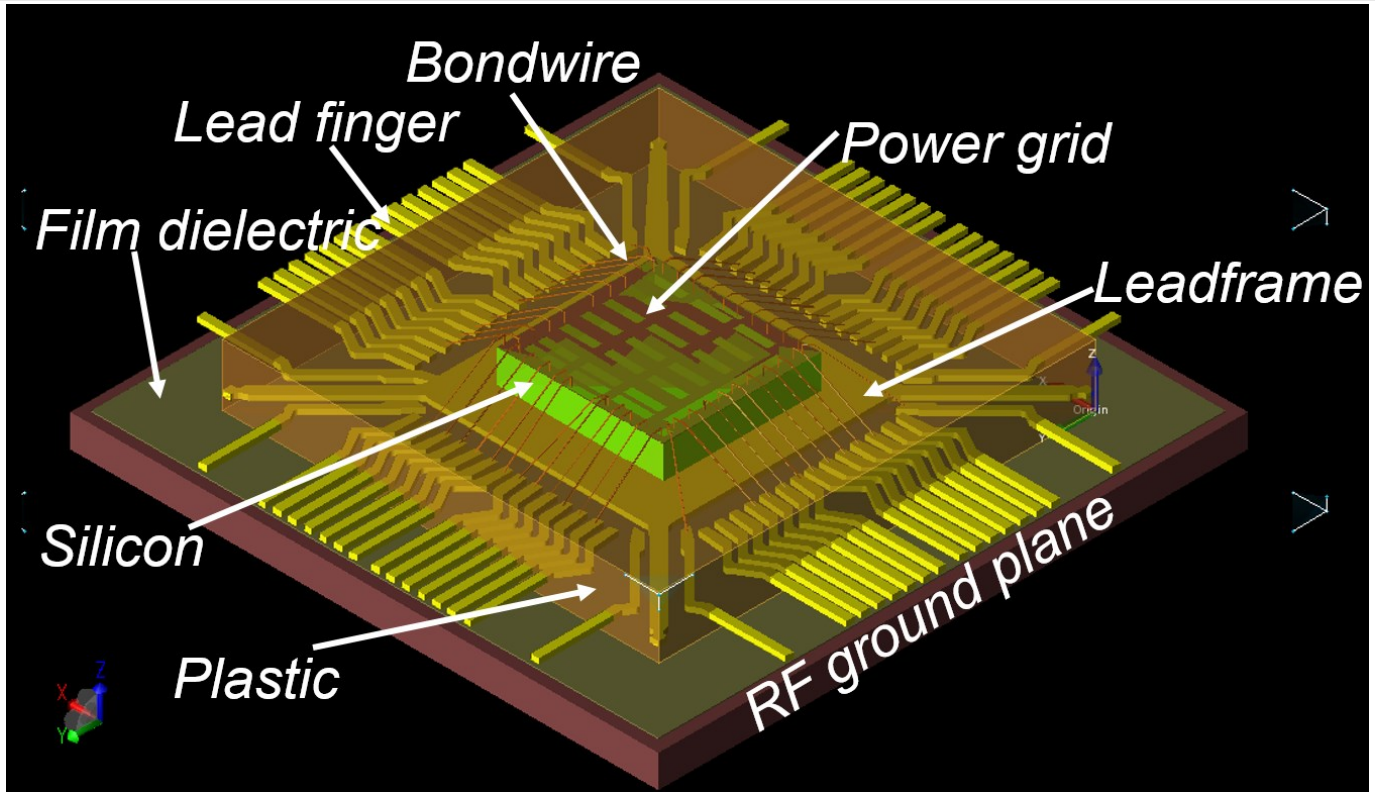
CDM Simulations: Substrate Modeling





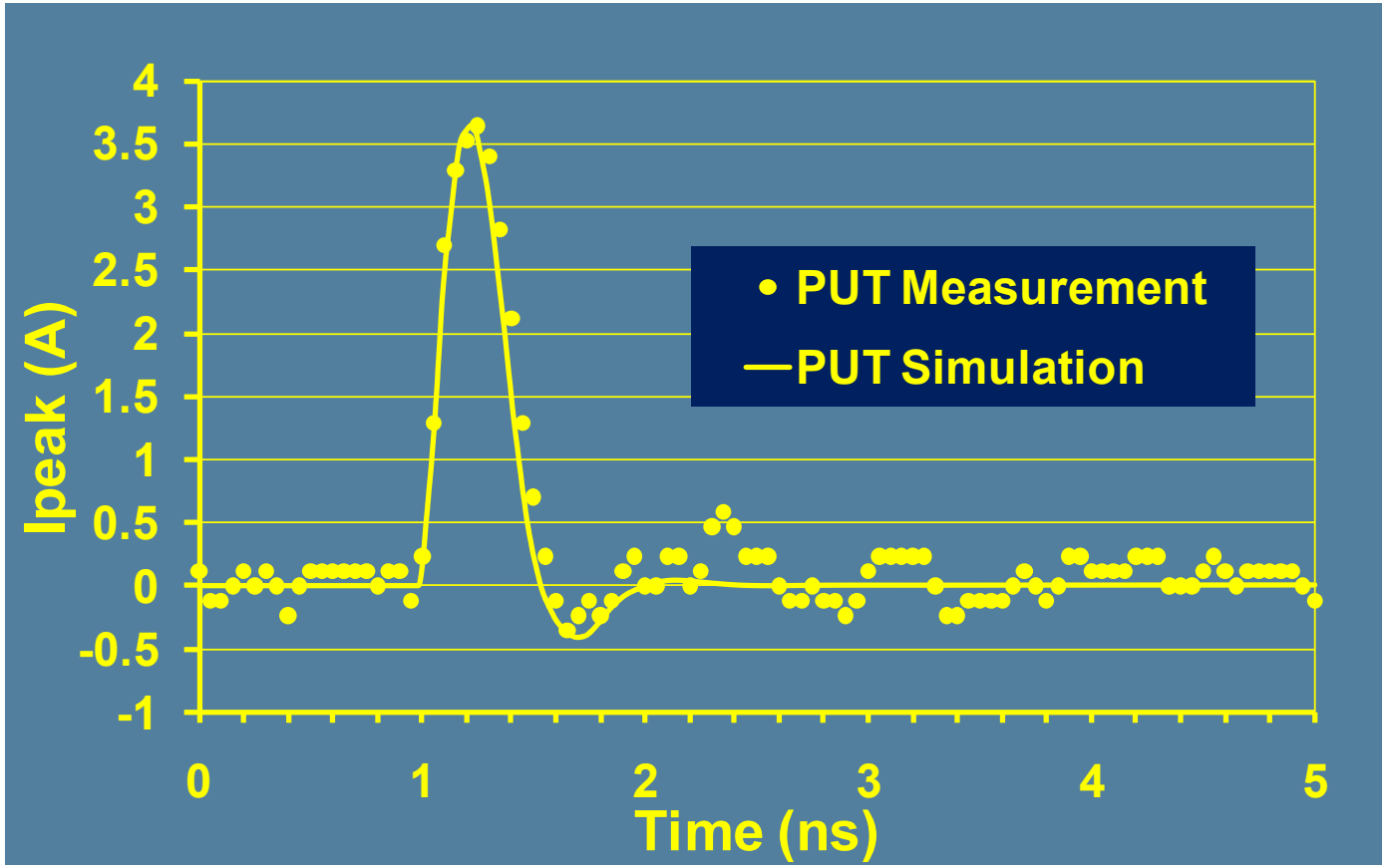
- A 3.5mm x 3.3mm Silicon Tuner IC processed in an NXP proprietary BiCMOS technology
- The substrate coupling of the die is extracted with a 3D high frequency electromagnetic solver @ 1.1GHz

CDM Simulations: IC Package Model



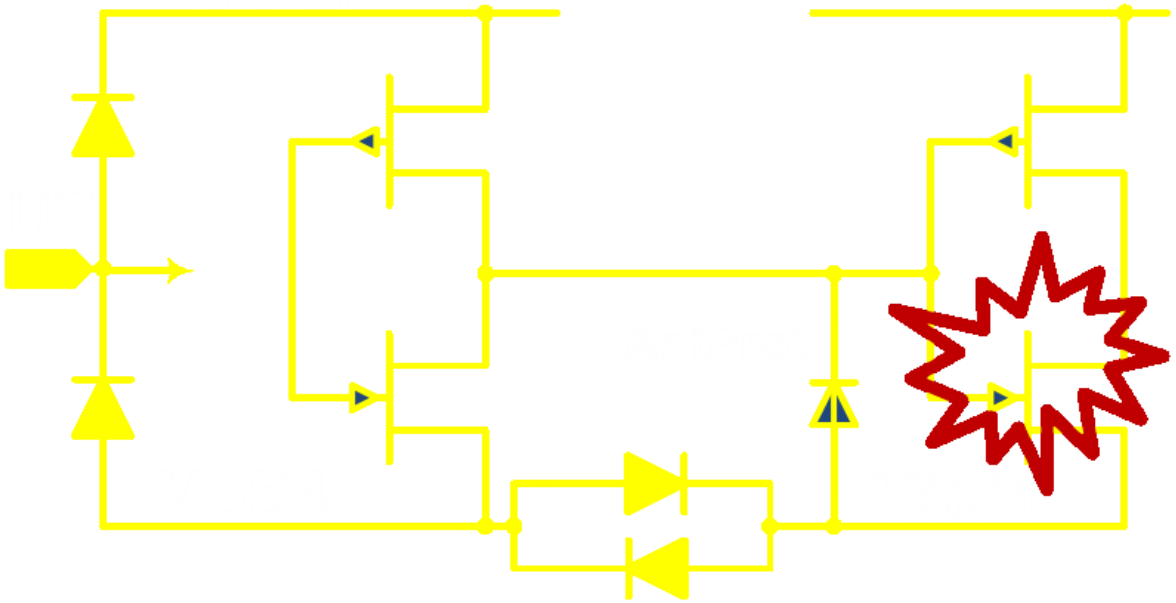
- IC package influences the CDM discharge significantly
- Accurate Spice simulation model required
- Based on Time Domain Reflectometry (TDR) measurements

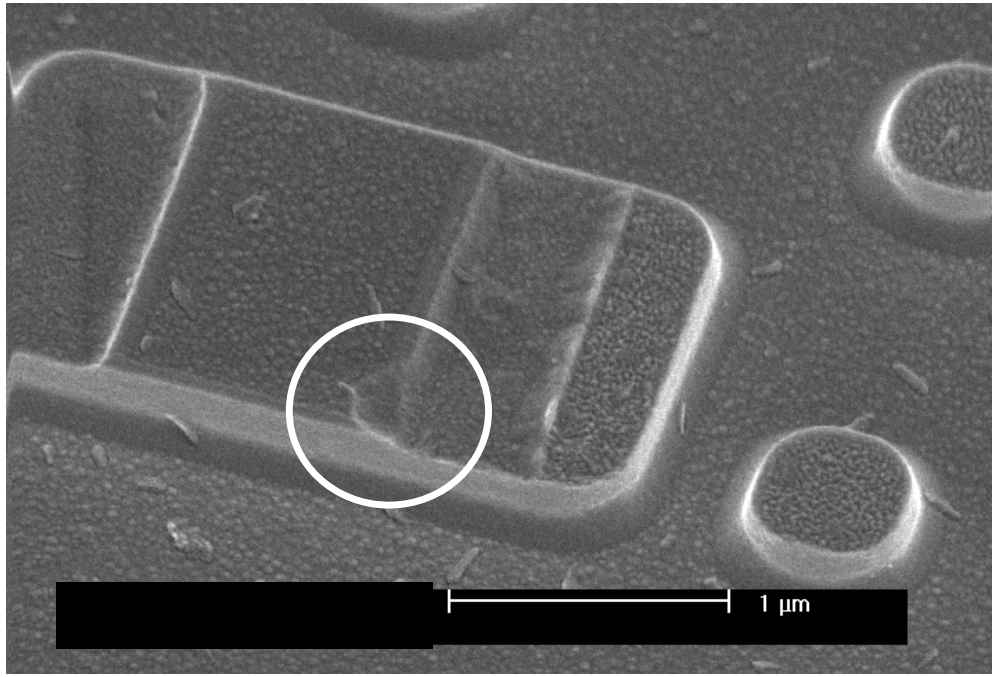
CDM Discharge Simulations



- Good agreement simulation and measurement
- R_{ARC}= 30Ω arc impedance (used as fitting parameter for Ipeak)

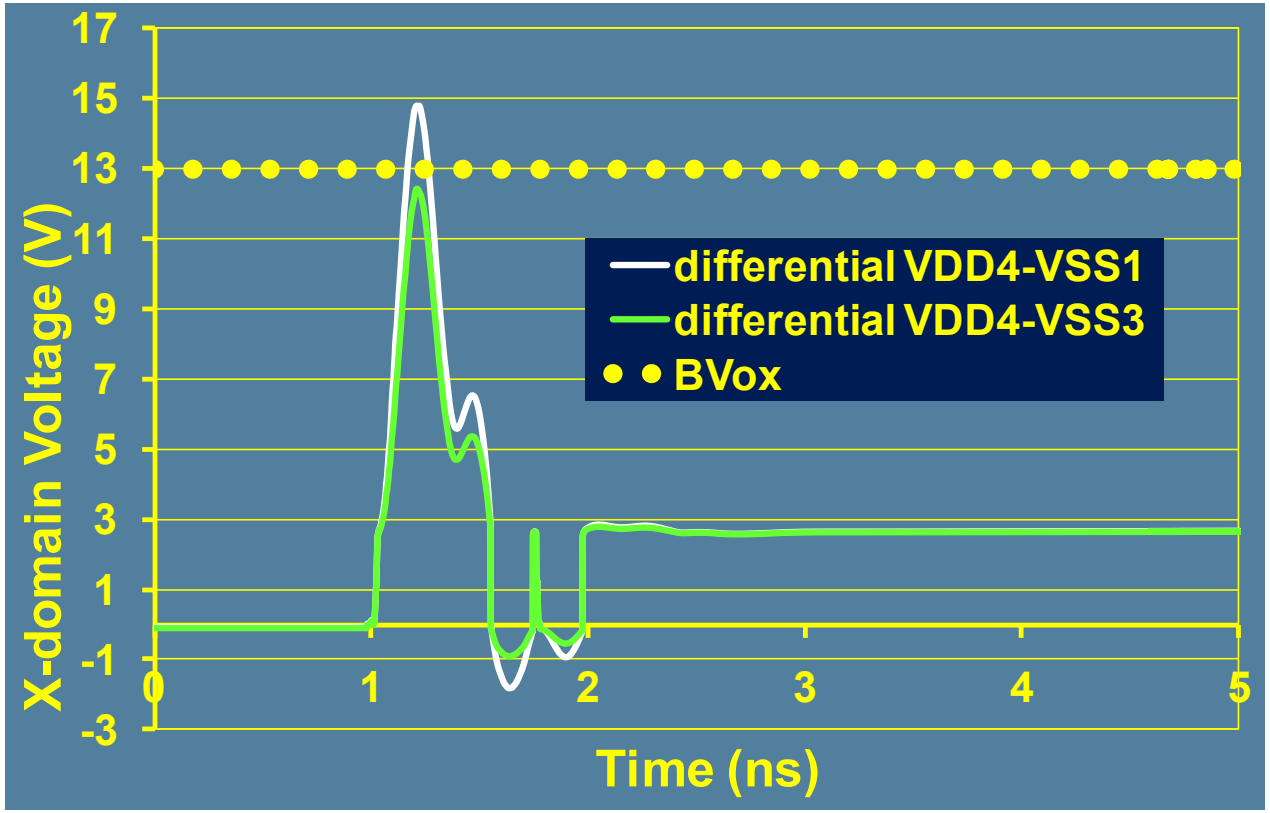
Cross-Domain CDM Fail





- Failure mode: passed 400V but failed -500V
- Gate-source defect in an NMOST ➔ cross-domain circuit VDD4-VSS1
- Antenna diode does not prevent CDM failure
- Note: The central ESD clamp is not shown

Cross-Domain Voltage Simulation



- Simulation explains
  - **Failure mode (Gate oxide breakdown)**
  - **No CDM X-domain failure in VDD4-VSS3**
- The failure mode was fixed
- A local CDM clamp was added in parallel to the antenna diode

CONCLUSIONS

Conclusions

- The HBM simulations have been silicon calibrated successfully and are useful:
  - to verify ESD design guidelines are met
  - to highlight weak areas of IC designs
  - to report current density violations and high resistance paths
- This predictive CDM simulation method is efficient to:
  - understand the CDM discharge mechanism in IC's
  - improve the predictability of CDM robustness of the IC's
- ESD Layout Check Tools are applied, implemented and used for RF IC designs before tape-out within NXP Semiconductors

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